Instability in Half-Bridge Circuits Switched With Wide Band-Gap Transistors

Andrew Lemmon, *Member, IEEE*, Michael Mazzola, *Member, IEEE*, James Gafford, *Member, IEEE*, and Christopher Parker, *Student Member, IEEE*

***Abstract*—Wide band-gap (WBG) field-effect devices are known to provide a system-level performance benefit compared to silicon devices when integrated into power electronics applications. However, the near-ideal features of these switching devices can also introduce unexpected behavior in practical systems due to the presence of parasitic elements. The occurrence of self-sustained oscillation is one such behavior that has not received adequate study in the literature. This paper provides an analytical treatment of this phenomenon by casting the switching circuit as an unintentional negative resistance oscillator. This treatment utilizes an established procedure from the oscillator design literature and applies it to the problem of power circuit oscillation. A simulation study is provided to identify the sensitivity of the model to various parameters, and the predictive value of the model is confirmed by experiment involving two exemplary WBG devices: a SiC vertical-channel JFET and a SiC lateral-channel MOSFET. The results of this study suggest that susceptibility to self-sustained oscillation is correlated to the available power density of the device relative to the parasitic elements in the circuit, for which wide band-gap devices, to include SiC and GaN transistors, are in a class approaching that of the radio frequency domain.**

***Index Terms*—Gallium nitride, natural response, oscillation, silicon carbide, stability.**

I. Introduction

RECENT advances in the maturity of wide band-gap (WBG) semiconductors have increased the likelihood that power electronics applications will begin to integrate this technology on a large scale in the new few years, as designers continue to push for ways to improve the efficiency and power density of their systems. Compared to their silicon counterparts, WBG field-effect transistors are characterized by reduced conduction losses, reduced switching losses, increased blocking voltage, increased operating frequency, and increased tolerance to junction temperature. When these devices are properly designed into power electronics applications, their device-level performance advantages are known to produce a measurable system-level benefit in terms of efficiency and power density [1]. These system-level benefits are unlocked, in large measure, due to the fast-switching characteristics of WBG devices, which permit operation at high frequency without excessive switching losses. However, the same fast-switching properties that enable this system-level benefit can have other less desirable side-effects as well. One commonly reported complication encountered in design of systems with WBG devices is the presence of an undesirable level of under-damped natural response in the application circuit [2]–[7]. The primary reason for this pronounced natural ring-down is the switching characteristics of the WBG transistors employed in these designs. As the switching behavior of practical devices approaches that expected from the die dimensions at the unipolar limit of SiC and GaN transistors, the $\mathrm{d}V/\mathrm{d}t$ and $\mathrm{d}I/\mathrm{d}t$ observed during switching transients increases, and the amount of stray inductance in the power circuit necessary to produce troublesome dynamics (ringing and oscillation) is reduced. For this reason, applications incorporating high-performance, fast-switching WBG devices should be designed in a manner that accounts for the consequences of greater sensitivity to stray inductance. A second anomaly that can occur in circuits based on WBG devices is the occurrence of unintended switching events. In a half-bridge circuit, this behavior can manifest itself as shoot-through when the active switch turns on. In this case, $\mathrm{d}V/\mathrm{d}t$ induced displacement current flows through the Miller capacitor into the gate drive of the inactive switch, which will result in Miller turn-on if the gate node rises to threshold. Alternatively, unintended turn-on can result from an uncommanded rise in the gate–source voltage produced by negative $\mathrm{d}I/\mathrm{d}t$ through the common source inductance during the turn-off of the actively gated switch. WBG-based systems are known to be at increased risk to both these sources of inadvertent switching due to their fast switching times [8]. One further switching-related anomaly that has not received adequate study in the literature is the possibility of self-sustained oscillation in circuits based on WBG devices. An experimental example of this behavior observed in a SiC-based half bridge is shown in Fig. 1, and the circuit used to generate these waveforms is presented in Fig. 2. It should be noted that the self-sustained oscillation phenomenon reported in this paper is not caused by re-triggering of the gate-drive PWM

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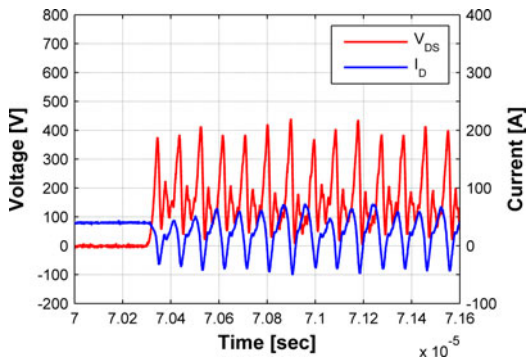

Fig. 1. Half-bridge turn-off showing self-sustained oscillation. The initial load current for this experiment was approximately 40 A.

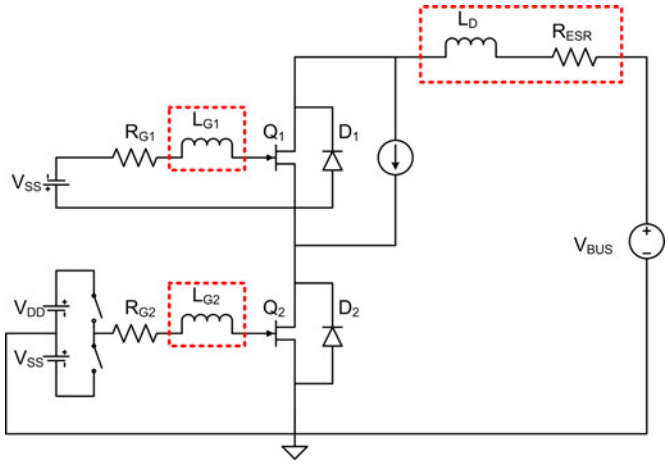

Fig. 2. Clamped inductive load test circuit used to generate waveforms in Fig. 1. Parasitic elements are outlined with dashed boxes. Note that the top switch is not actively gated, but is biased OFF. The clamped inductor is represented as a current source.

signal. The occurrence of self-sustained oscillation is distinct from both the underdamped natural ring-down and the occurrence of shoot-through. This distinction can be made primarily on the basis of the fact that self-sustained oscillation is a perpetual phenomenon, whereas the other two anomalies are transient events. Although the occurrence of natural ring-down or of shoot-through can in some cases act as a "triggering" mechanism leading to the onset of self-sustained oscillation, the governing relationships that underlie these phenomena are quite different and independent treatment is therefore warranted. Since the occurrence of natural-ring down and shoot-through have been sufficiently addressed in the WBG device literature, the current work focuses exclusively on the third identified switching anomaly, namely the possibility of self-sustained oscillation.

II. Literature Review

The phenomenon of self-sustained oscillation in circuits based on WBG semiconductors has not received a detailed treatment in the literature at the time of this writing. Nevertheless, occurrences of this problem have been reported several times in the literature, and most of these reports have occurred during the last one or two years as WBG device adoption has accelerated. For example, Rodriguez *et al*. [9] report the occurrence of self-sustained oscillation of GaN FETs during switching characterization. Danilovic *et al*. [10] also report a switching characterization effort with GaN devices that encountered self-sustained oscillation. Both SiC and GaN device manufacturers have also made reference to this phenomenon in their application literature. In a recent seminar by Efficient Power Conversion Corporation (EPC) [11], White report that gate-loop inductance present in GaN-based applications "can easily make an oscillator". In an EPC application note [12], Abdoulin *et al*. warn potential customers about the possibility of self-sustained device oscillation during pulsed curve tracer measurements. Other EPC application materials by Abdoulin *et al*. [13] and Strydom [14] further reinforce these warnings regarding self-sustained oscillation and recommend minimizing the gate-loop inductance through careful layout and the use of the strip-line impedance matching design technique. Texas Instruments informs users about the possibility of gate-loop oscillation in the datasheet for its recently released GaN gate-drive IC, the LM5113 [15]. Cree warns of the possibility of self-sustained oscillation in a recent application note [16] and in the datasheet for the recently released 1200 V, 100 A SiC MOSFET module [17]. None of these papers presents a detailed treatment of the self-sustained oscillation phenomenon. Instead, these works serve primarily to notify application designers of the possibility of this phenomenon and provide experience-based hints for mitigation when this problem is encountered.

Several other studies provide context relevant to the current paper, even though they do not explicitly reference the self-sustained oscillation phenomenon. For example, two papers by Chen *et al*. [18], [19] provide an empirically based analysis of the parasitic elements that contribute to the pronounced natural ring-down in WBG applications. Other studies of the natural ring-down phenomenon are provided by Josifovic *et al*. [20] and Adamowicz *et al*. [21]. All of these papers indicate that the primary method available to designers for managing the natural ring-down phenomenon is the reduction of switching speed. Indeed, two additional papers go so far as to claim that the aggregate inductance of the gate loop establishes a practical limit to the switching frequency achievable in hard-switched applications [22], [23]. This is an important observation, as it reinforces the claim that high switching speed brings with it increased risk to the occurrence of various switching anomalies, of which self-sustained oscillation is an example. Analytical expressions for the natural ring-down phenomenon in the power loop are provided by Alatise *et al*. [24] and Wang *et al*. [25]. The former paper is concerned primarily with the contribution of the anti-parallel diode to power loop natural ring-down. The expressions provided in the latter paper are more relevant to the current paper, as they are based on an equivalent circuit that includes MOSFET intrinsic capacitances. However, [25] excludes consideration of the gate-loop inductance, which renders it inadequate to the task of describing the self-sustained oscillation phenomenon. Both [26] and [8] provide detailed analytical treatments of the shoot-through switching anomaly, along with threshold criteria to avoid this behavior by reducing either switching speed or gate-loop parasitic inductance. Neither

of these sources attempts an analytical treatment of the natural ring-down or self-sustained oscillation phenomena, but the equivalent circuit models used by both could serve as a basis for such a treatment. Finally, in [27], Fujihira *et al*. present a theoretical treatment of a mode of parasitic-induced oscillation observed during turn-off of a fast-switching silicon MOSFET. In this paper, even though the possibility of self-sustained oscillation is not mentioned, the presented treatment follows a similar methodology to that employed in the current paper. However, in order to reduce the complexity of the analytical treatment, the authors of [27] exclude consideration of the device gate-drain capacitance. The gate-drain capacitance represents an important intrinsic feedback mechanism present in any field-effect device that significantly influences the stability of FET-based half-bridge circuits. This simplification limits the utility of the analysis presented in [27] for predicting the possibility of half-bridge instability and makes it impossible to predict the bus voltage dependence of any observed oscillatory phenomena.

Several other papers that deal with switching anomalies in WBG-based systems may actually serve to perpetuate a general confusion regarding this topic. For example, in [28], Delaine *et al*. describe the design of a 1 MHz buck converter based on GaN devices that experiences several inter-related oscillatory phenomena. Although it appears that the root cause of these problems is parasitic-induced oscillation, the authors refer to the occurrence of EMC perturbation and radiated emissions as the suspected cause. In another recent paper [29], Noguchi *et al*. also present an analysis of the oscillatory modes observed in a 1 MHz half-bridge inverter. The authors conclude that the 80 MHz ringing observed in the system is the result of common mode noise capacitively coupled into the gate drive circuit. While this is undoubtedly a contributing factor to the observed problems, there is also a significant measure of parasitic-induced oscillation that goes unexplained. In [30], Watanabe *et al*. provide an analysis of both the natural ring-down and shoot-through phenomena observed in a half-bridge switching test circuit. Unfortunately, the analysis in this paper does not cleanly separate these two phenomena and the result may be somewhat confusing to the reader. None of these papers deals with the phenomenon of self-sustained oscillation, although evidence of related oscillatory phenomena is visible in each.

It should be noted that susceptibility to self-sustained oscillation is correlated with the performance of the WBG device being employed. As Kaminski and Hilt report in [31], current-generation GaN HFETs and SiC vertical-channel JFETs are the only commercially available WBG devices with performance approaching the 4 H SiC unipolar limit. These two categories also represent the devices that are most commonly reported to experience self-sustained oscillation. Thus, the WBG devices with the highest-available performance are also the devices with the greatest susceptibility to self-sustained oscillation. This can be explained in part by the very low specific on-resistance of these devices. The small die size of these devices results in support for very fast switching: SiC vertical channel JFETs were recently reported to switch 20 A at 600 V at speeds of greater than 30 V/ns [32]; GaN HFETs were recently reported to switch 20 A at 350 V at speeds of 80 V/ns [7]. Commercially available SiC lateral-channel MOSFETs, on the other hand, have reduced susceptibility to self-sustained oscillation. The comparably higher specific on-resistance of this topology means that practical devices have larger die area than similarly rated SiC vertical-channel JFETs and GaN HFETs [1], [33], [34]. The comparably higher intrinsic capacitance of the SiC lateral channel MOSFET not only reduces the switching speed available to applications with similar gate drive capability, but also provides a self-snubbing effect that serves to further reduce susceptibility to self-sustained oscillation, at the cost of increased switching losses and/or gate drive power. Nevertheless, the lateral channel SiC MOSFET is not immune as this device has been reported to experience self-sustained oscillation as well [16], [17].

III. Theoretical Analysis

In order to provide a means by which power electronics practitioners can deterministically eliminate the possibility of self-sustained oscillation from occurring in their applications, a comprehensive theoretical treatment of this phenomenon is required. One reference that provides a qualitative description of the natural ring-down phenomenon does so by breaking down this behavior into two components: (1) the initial storage of energy in the power loop resonant tank, which is observable as a voltage overshoot, and (2) the damped oscillatory ring-down as this energy storage is dissipated in the power loop equivalent series resistance [35]. Although the mechanisms that govern the self-sustained oscillation are different from this description, this compartmentalization of the resonant behavior is attractive for describing the self-sustained oscillation phenomenon as well. One reason why this is true is that the underlying conditions that enable these two modes appear to be separate. As will be described in Section V, it is possible to create an initial cycle that is favorable to self-sustained oscillation without creating a self-sustained oscillator. This compartmentalization also permits the analysis of the second phase of oscillation to occur at a higher level of abstraction, which is in agreement with an established construct found in the literature. Therefore, this logical separation of this behavior into an initial cycle and the subsequent oscillatory behavior will be adopted for the remainder of this paper following the analytical treatment first published by the authors in [36]. The previous work represented a special case applicable to SiC JFETs that exhibit negligible drain–source capacitance. The formulation presented here is generalized to include the effect of drain–source capacitance, and is therefore applicable to any field-effect device, without regard for device topology.

A. Initial Cycle

The behavior of the clamped-inductive-load test circuit of Fig. 2 during the initial cycle of oscillation can be understood by considering the simplified equivalent circuit shown in Fig. 3. A positive $\mathrm{d}V/\mathrm{d}t$ is expressed across the drain and source terminals of the active switch when it is gated off; a similar voltage slew is seen by the inactive switch in a half-bridge circuit when the active switch is gated on. In either case, this positive $\mathrm{d}V/\mathrm{d}t$ causes displacement current (I_G) to flow through the Miller

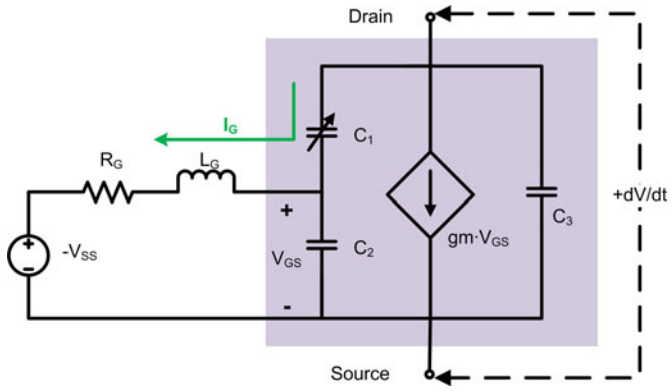

Fig. 3. Equivalent circuit of power FET during positive $\mathrm{d}V/\mathrm{d}t$ event at turn-off.

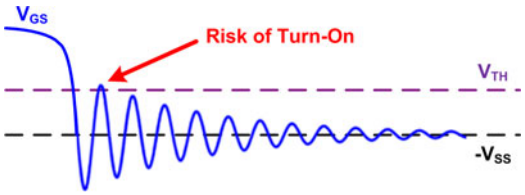

Fig. 4. Notional gate–source ring-back to threshold during initial cycle of natural ring-down.

capacitance (C_1) of the device with the polarity indicated in Fig. 3. This displacement current must be sunk by the gate drive in order to prevent inadvertent turn-on of the device. During this process, the gate inductance (L_G) stores energy, which must be dissipated in order for the gate–source voltage to settle at the gate-drive low-line potential $(-V_{\mathrm{SS}})$. The presence of nonnegligible device input capacitance as represented (primarily) by C_2 means that the gate–source voltage will exhibit a second-order ring-down as the resonant tank formed by L_G and C_2 is depleted of energy by dissipation in the gate resistor (R_G). It is important to recognize that WBG circuits intended for fast switching typically utilize a small R_G value. There are two reasons for this. First, a small R_G value is required to enable rapid charging and discharging of the FET input capacitance. Second, a small value for R_G also reduces the susceptibility of the circuit to Miller turn-on because it improves the ability of the gate-drive circuit to quickly sink displacement current. However, the selection of a small R_G value has an additional unintended side-effect: it results in an underdamped gate loop in the presence of any stray gate inductance. As a result, the positive $\mathrm{d}V/\mathrm{d}t$ event that occurs during every switching cycle has the potential to produce an underdamped gate-loop natural ring-down. When this occurs, the first time the gate–source voltage rings back above $-V_{\mathrm{SS}}$ there is the possibility that the gate potential may reach the threshold voltage and the device may turn back on, as depicted in Fig. 4. The resulting channel conduction creates an additional current path, which is represented by the dependent current source in Fig. 3. If ring-back falls short of the threshold voltage, then self-sustained oscillation is not possible. If ring-back to threshold occurs, then the resulting channel conduction will distort the natural response of the two-mesh circuit such

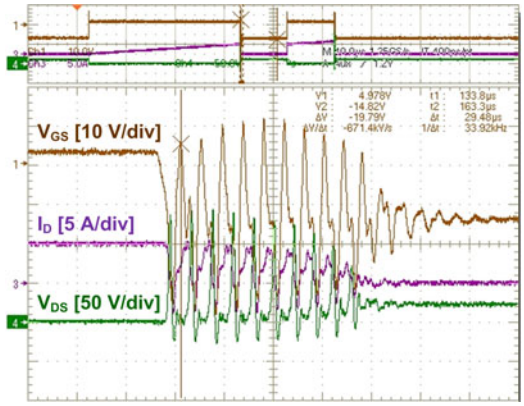

Fig. 5. Burst of forced cycles that self-extinguish at a bus voltage of 20 V.

that the next cycle is also likely to reach threshold as well. Thus, the possibility that the gate–source voltage may ring back to the device threshold voltage and cause unintended channel conduction is an important condition that satisfies the bias conditions necessary to apply the small signal model presented in the next section.

A cycle during which the gate–source voltage rings back to threshold and causes channel conduction to occur is referred to hereafter as a "forced" cycle. As will be seen in Section V, forced cycles have several attributes that distinguish them from cycles associated with the natural ring-down of the gate-loop ("natural" cycles). In addition to the sudden changes in drain current and drain–source voltage that accompany the onset of channel conduction, the gate–source voltage is usually observed to remain near the device threshold during the duration of the forced cycle. The period of a forced cycle is also typically two to three times longer than a natural cycle, due to the delay caused by channel conduction. The occurrence of a forced cycle during the initial gate–source voltage ring-back is dependent on several factors: the drain–source voltage slew rate, the $C_{\mathrm{ISS}}/C_{\mathrm{RSS}}$ ratio of the device, the amount of stray gate-loop inductance, and the voltage headroom between $-V_{\mathrm{SS}}$ and the device threshold voltage. The likelihood of a forced cycle is also dependent on the bus voltage and the magnitude of the drain current prior to the turn-off event. The development of a validated theoretical treatment of this portion of the self-sustained oscillation phenomena is an ongoing research effort that is planned for a future paper.

B. Continuance of Self-Sustained Oscillation

The presence of a forced cycle is a necessary but not a sufficient condition to determine whether self-sustained oscillation is likely to occur. This can be understood by considering the experimental results shown in Figs. 5 and 6. These results correspond to operation of the inductively loaded switching test circuit of Fig. 2 with depletion-mode SiC JFETs and the gate-drive circuit described in [37]. The oscillogram of Fig. 5 contains at least ten forced cycles, but this oscillation eventually self-extinguishes. Fig. 6, on the other hand, demonstrates a sequence of perpetual forced cycles that comprise an instance of self-sustained oscillation. The operating conditions for these two experiments were

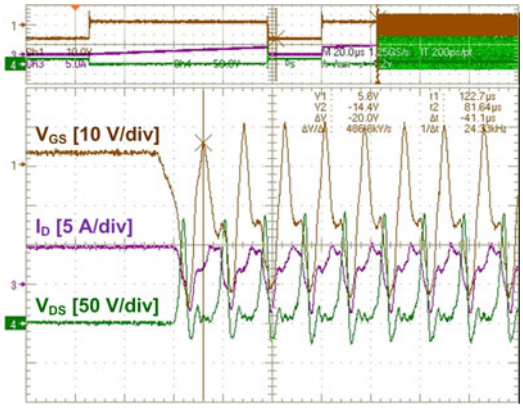

Fig. 6. Sequence of forced cycles comprising an instance of self-sustained oscillation at a bus voltage of 25 V.

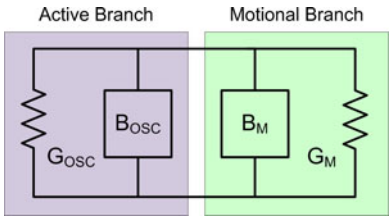

Fig. 7. Notional small-signal model for negative conductance oscillator.

identical with the exception of the bus voltage applied. It can be concluded that some additional mechanism beyond the presence or absence of forced cycles is necessary in order to predict the possibility of self-sustained oscillation.

In contrast to the occurrence of a damped natural-response, the phenomenon of self-sustained oscillation cannot be attributed solely to the exchange of energy between parasitic elements. The self-sustaining nature of the oscillation shown in Fig. 6 implies that the energy dissipated by parasitic resistance in the circuit during each cycle is replaced by a feedback mechanism drawing energy from the bus. An established conceptual framework for describing this process common in the oscillator design community is the negative resistance (or negative conductance) model [38], [39]. One of the contributions of the current paper is the recognition that the WBG field-effect device and its associated parasitic elements can be re-cast as an unintentional negative-resistance oscillator. The advantages of this approach are that it leverages a well-established formalism for describing the propensity of a circuit to oscillate indefinitely, and it provides a higher level of abstraction that is useful for making predictions about practical power electronics applications.

According to the negative conductance formulation, the oscillator is represented as a single port network composed of two-branches: a "motional" branch and an "active" branch. In the case of a traditional linear oscillator circuit, the motional branch is implemented with a crystal, and the active branch is implemented with a transistor and an appropriate bias circuit. This abstraction of the notional oscillator circuit is shown in Fig. 7. As a practical matter, the operation of the notional oscillator can be understood by recognizing that susceptances B_{OSC} and B_M collectively form a resonant tank and the positive conductance G_M extracts energy from this tank during each cycle of oscillation. The "negative conductance" represented in the active branch is a circuit that is capable of adding energy back to the resonant tank from an external source. Negative conductance is a convenient abstraction that permits the overall stability of this circuit to be described in terms of energy transfer rather than through circuit analysis methods.

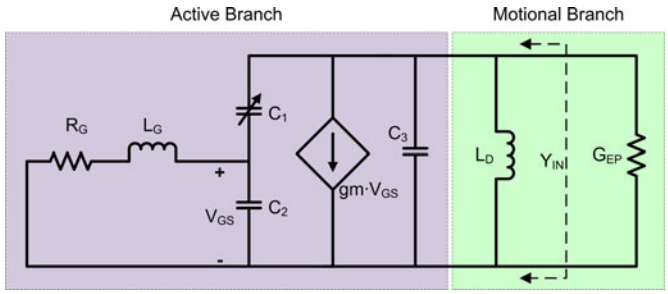

Fig. 8. Small-signal model of unintentional WBG transistor oscillator.

In order for the notional two-branch oscillator shown in Fig. 7 to achieve constant-envelope oscillation, the following two conditions must be satisfied: 1) the susceptance in the motional branch must be canceled by an opposite-signed and equal-magnitude susceptance in the active branch ($B_M = -B_{\mathrm{OSC}}$); and 2) the positive conductance in the motional branch must be canceled by an equal-magnitude negative conductance in the active branch ($G_M = -G_{\mathrm{OSC}}$). In the oscillator design literature, small-signal models are commonly used to predict the occurrence of self-sustained oscillation at a given operating point by evaluating these two criteria [39], [40]. In the case of the unintentional WBG transistor oscillator, the physical circuit shown in Fig. 2 can be abstracted into a small-signal negative conductance oscillator model suitable for the application of this analysis procedure. This is accomplished by removing independent voltage and current sources and reflecting the power loop parasitic components L_D and R_{ESR} as parallel equivalents, assuming that $\omega L_D \gg R_{\mathrm{ESR}}$. In the case of the high-side switch, the anti-parallel rectifier clamps the current source following turn-off of the low-side switch and thus is a short circuit in the small signal model. The small-signal model that results from this process is shown in Fig. 8. In this representation, the active branch is represented by the equivalent circuit of the WBG transistor and its associated gate drive circuit; the motional branch is represented by the power loop parasitic elements. With the independent sources removed, the reactance of the power loop is predominantly inductive, while the reactance of the active branch is predominantly capacitive.

By considering the admittance seen from Y_{IN}, it can be seen that satisfying the first condition for oscillation implies that $Im\{Y_{\mathrm{IN}}\} = 0$ since Y_{IN} incorporates the reactive portions of both motional and active branches. This relationship is satisfied at one or more frequencies, which represent the resonant modes of the system. Satisfying the second condition for constant-envelope oscillation implies that $Re\{Y_{\mathrm{IN}}\} = -G_{\mathrm{EP}}$. This condition determines the envelope of oscillation. In practice, evaluation of the second condition is what determines whether the

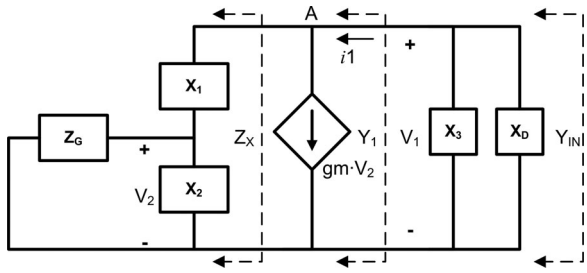

Fig. 9. Annotated small-signal WBG oscillator equivalent circuit.

WBG oscillator will sustain oscillation or not. Three possibilities can result from the evaluation of this second condition. When $Re\{Y_{\rm IN}\} > -G_{\rm EP}$, the model predicts an oscillation envelope with decreasing magnitude over time; when $Re\{Y_{\rm IN}\} = -G_{\rm EP}$, the model predicts constant-envelope oscillation; and when $Re\{Y_{\rm IN}\} < -G_{\rm EP}$, the model predicts an oscillation envelope with increasing magnitude over time. However, in practice, it is found that the unintentional WBG oscillator will either experience self-extinguishing oscillation if insufficient negative conductance is available $(Re\{Y_{\rm IN}\} > -G_{\rm EP})$ or self-sustained oscillation if sufficient negative conductance is available $(Re\{Y_{\rm IN}\} \leq -G_{\rm EP})$. The increasing-envelope case ultimately collapses into the constant-envelope case because nonlinearities present in a practical circuit prevent the amplitude of oscillation from increasing indefinitely. This automatic establishment of equilibrium is a well-known principle that is relied upon in intentional oscillator design to ensure proper oscillator start-up [38].

An analytical expression for $Y_{\rm IN}$ can be readily derived by considering the annotated form of the small signal model presented in Fig. 9. In this form, the following equalities are established: $X_1 = 1/(j\omega C_1), X_2 = 1/(j\omega C_2), X_D = j\omega L_D$, and $Z_G = R_G + j\omega L_G$.

First, an expression for Z_X is created

$$Z_X = X_1 + \frac{Z_G X_2}{Z_G + X_2}. \tag{1}$$

The voltage across X_2 is then found by voltage division

$$V_2 = V_1 \cdot \frac{Z_G X_2/(Z_G + X_2)}{X_1 + Z_G X_2/(Z_G + X_2)}. \tag{2}$$

Writing Kirchhoff's current law (KCL) for the node labeled "A" produces the following expression:

$$-i_1 + g_m V_2 + \frac{V_1}{Z_X} = 0. \tag{3}$$

Substituting (3) into an expression for Y_1 produces the following result:

$$Y_1 = \frac{I_1}{V_1} = g_m \frac{V_2}{V_1} + \frac{1}{Z_X}. \tag{4}$$

Substituting (1) and (2) into (4) and multiplying by $(Z_G + X_2)/Z_G X_2$ yields the following result:

$$Y_1 = \frac{g_m + ((Z_G + X_2)/Z_G X_2)}{X_1 (Z_G + X_2)/Z_G X_2 + 1}. \tag{5}$$

Finally, the expression for $Y_{\rm IN}$ can be obtained by combining Y_1 with X_3 and X_D:

$$Y_{\rm IN} = \frac{g_m + (Z_G + X_2)/Z_G X_2}{X_1 (Z_G + X_2)/Z_G X_2 + 1} + \frac{1}{X_3} + \frac{1}{X_D}. \tag{6}$$

Equation (6) can be used to determine the susceptibility of a particular circuit to self-sustained oscillation by following a two-part analysis procedure. The resonant frequency of the circuit is first determined by solving for the roots of the equation $Im\{Y_{\rm IN}\} = 0$. For the general case of (6) in which none of the components are negligible, separating the imaginary portion of $Y_{\rm IN}$ produces a cubic equation in terms of ω^2. Thus, three independent solutions for $|\omega|$ are possible, and each solution is a valid resonant frequency for the small-signal model. However, it has been determined through empirical analysis that the solution that matches the observable resonant frequency of the circuit is the lowest of the three solutions. Once the applicable resonant frequency is determined, this value is substituted into $Re\{Y_{\rm IN}\}$ and the result is compared to $-G_{\rm EP}$. If $Re\{Y_{\rm IN}\} \leq -G_{\rm EP}$, the specified set of circuit parameters is predicted to produce self-sustained oscillation.

The model presented here is flexible enough to provide useful information to designers regarding the propensity of practical circuits to experience self-sustained oscillation. Since this predictive ability is based on a small-signal model, it is by definition dependent upon the selection of an operating point. However, the operating conditions of the circuit are not explicitly represented in the formulation given by (6), so it may not be immediately apparent how an operating point is chosen for analysis. This is done implicitly through the selection of circuit parameter values. For instance, the Miller capacitance of a field effect device is known to be a nonlinear function of the drain–source voltage. Therefore, model value C_1 is chosen to represent the Miller capacitance associated with a particular WBG device linearized around a particular drain–source bias. Likewise, the model values C_2 and g_m are selected to represent linearized values for a given device around a gate–source voltage bias near the threshold voltage. The operating point dependence of the model does not limit its utility for predicting the likelihood of self-sustained oscillation across a wide range of operating points. One reason is the physical reality of this quasi-static condition imposed by the nature of the circuit involved, which is a half-bridge switching a clamped inductive load on a constant voltage bus. The oscillation in question occurs after commutation of the switch current to the opposite leg of the half bridge where the central tendency of the oscillating drain source voltage is the bus value. A second reason is that the gate–source voltage is clamped at or near the threshold voltage by displacement current flowing through the Miller capacitance when the channel begins to conduct; a fact empirically established in Section V. The implementation used by the authors incorporates a look-up table of Miller capacitance values vs. drain–source bias for several specific WBG devices. By leveraging this information, a specific set of circuit parasitic values can be evaluated across a range of drain–source voltages to determine susceptibility to self-sustained oscillation as a function of voltage.

TABLE I
PARAMETER VALUES FOR SIMULATION STUDY

Parameter	SiC JFET	SiC MOSFET
L_G	100 nH	520 nH
L_D	300 nH	480 nH
G_{EP}	1.25 mS	1.81 mS
C_2 (near V_{GS}=V_{TH})	900 pF	1.3 nF
C_3	-	700 pF
gm (near V_{GS}=V_{TH})	5-15 mS	5-15 mS
R_{G_NORM}	0.04-0.07	0.04-0.07
V_{DS} Range	0-600 V	0-600 V

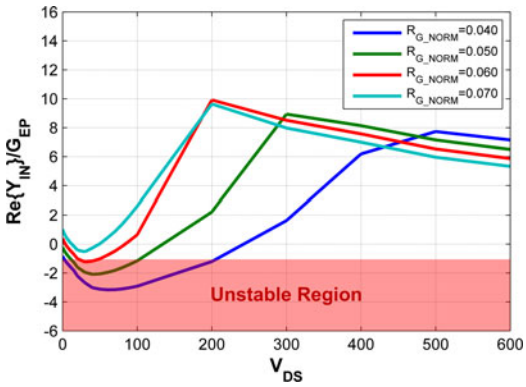

Fig. 10. Evaluation of R_{G_NORM} dependence for SiC JFET profile. Note that g_m is fixed at a nominal value of 10 mS.

IV. SIMULATION STUDY

As part of this paper, a simulation study was performed to evaluate the sensitivity of the model to various model parameters. It has been shown in a previous work that susceptibility to self-sustained oscillation increases with increased transconductance, and with reduced gate-loop damping expressed as the normalized gate resistance, $R_{G\_NORM} = R_G / \left[\sqrt{L_G/C_2}\right] = 2\zeta$, where ζ is the damping ratio of the gate loop [36]. In the current paper, the simulation study was designed to elucidate the implications of selecting a WBG transistor with a particular ratio of input capacitance to Miller capacitance. For this reason, the same simulation profile was executed with values corresponding to two test fixtures: one configured to evaluate a SiC JFET with a $C_{\rm ISS}/C_{\rm RSS}$ ratio of approximately 3 at 100 V drain–source bias, and one configured to evaluate a SiC MOSFET with a $C_{\rm ISS}/C_{\rm RSS}$ ratio of approximately 80 at 100 V drain–source bias. The specific parameter values used to populate the simulation for each test are presented in Table I.

In each of the following plots, the ordinate represents a normalized conductance figure of merit $Re\{Y_{\rm IN}\}/G_{\rm EP}$, which permits identification of the region of susceptibility to self-sustained oscillation. In these plots, any portion of the conductance curve that exists at or below the -1 point represents a region of susceptibility to self-sustained oscillation. The system sensitivity to the value of normalized gate resistance for the SiC JFET and the SiC MOSFET can be observed in Figs. 10 and 11, respectively. As anticipated from the previous work, both devices are more susceptible to self-sustained oscillation at small values of normalized gate resistance. However, the shape of the normalized conductance curves is instructive to compare. The SiC MOSFET, which has a higher $C_{\rm ISS}/C_{\rm RSS}$ ratio, creates a narrower region of susceptibility at a lower drain–source voltage than the SiC JFET. This is due to the fact that the higher $C_{\rm ISS}/C_{\rm RSS}$ ratio of the SiC MOSFET results in a scaling factor that compresses the normalized conductance curves toward lower drain–source voltage. A similar trend is evident in Figs. 12 and 13, which represent the system sensitivity to the value of FET transconductance for the SiC JFET and the SiC MOSFET, respectively. As anticipated from the previous work,

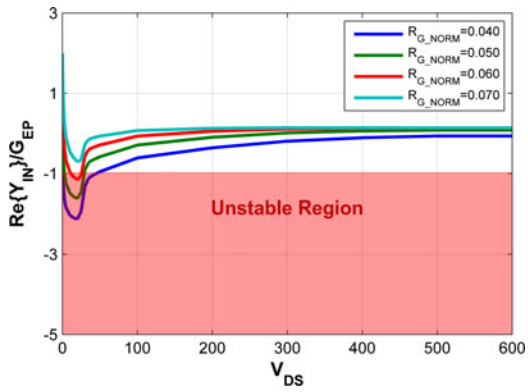

Fig. 11. Evaluation of R_{G_NORM} dependence for SiC MOSFET profile. Note that g_m is fixed at a nominal value of 7 mS.

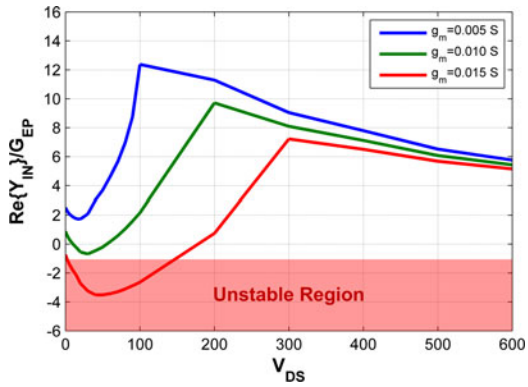

Fig. 12. Evaluation of g_m dependence for SiC JFET profile. Note that R_{G_NORM} is fixed at a nominal value of 0.068.

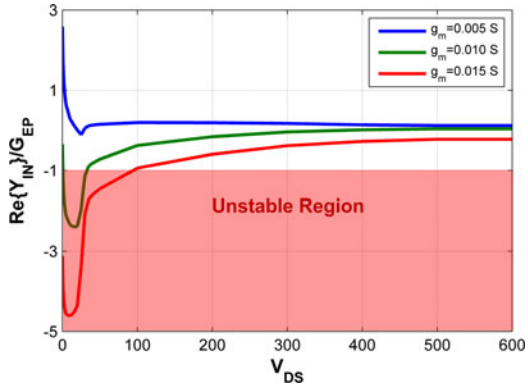

Fig. 13. Evaluation of g_m dependence for SiC MOSFET profile. Note that R_{G_NORM} is fixed at a nominal value of 0.060.

higher transconductance near threshold results in increased susceptibility to self-sustained oscillation. In addition, the same scaling trend is evident in the case of the SiC MOSFET, resulting in a narrower region of susceptibility at lower voltage when compared to the SiC JFET. However, it should also be noted that the SiC MOSFET creates a more gradual increase in normalized conductance with increased drain–source voltage at g_m values >5 mS. Thus, the SiC MOSFET could be described as having two separate regions of susceptibility: a severe region of susceptibility at low voltages, and a somewhat less severe but broader region of susceptibility at moderate voltages.

V. Empirical Study

As part of the current paper, an empirical study was conducted to evaluate the predictive performance of the small signal model presented in Section III. This effort consisted of executing a series of clamped-inductive-load tests using a switching circuit similar to that shown in Fig. 2. As in the previous section, both a SiC depletion-mode JFET and a SiC MOSFET were evaluated so that the device topology implications on the susceptibility to self-sustained oscillation could be validated. For the SiC JFET circuit, a gate-drive evaluation module available from the manufacturer was utilized [41]; for the SiC MOSFET circuit, the manufacturer's recommended gate-drive design was followed including layout suggestions [42]. No attempt was made to optimize the gate drive for either circuit beyond following the manufacturer recommendations. For each test circuit, the following procedures were utilized in order to determine the effective circuit values for use in populating the simulation. The effective power loop conductance $G_{\rm EP}$ was determined by direct observation of the damping ratio. Small coils of wire were used to construct L_D and L_G, which were characterized using a Wayne–Kerr precision magnetics analyzer and a custom test fixture suitable for the low inductance involved. The chosen values were selected in order to dominate over the stray inductance on the test board but are not unrealistic levels found in many applications [43]. The parameter that was used as a degree of freedom for curve-fitting purpose was the FET transconductance g_m. This parameter value cannot be considered to be firmly held constant for all tests, since device transconductance varies with gate–source voltage and the value of gate–source voltage ring-back varies slightly from test to test. However, the small range of values used for each device is known to be consistent with measured transconductance values at a gate–source voltage bias near the threshold voltage. The full set of parameter values that were measured in the two test fixtures and used to populate the corresponding simulations are given in Table II.

As has been pointed out in Section III, it is important that the initial cycle of oscillation establishes the bias conditions necessary to properly apply the small signal model upon which the susceptibility prediction is based. For this reason, a preliminary set of switching experiments was conducted in order to determine the conditions under which the initial cycle would establish the appropriate bias conditions. The two primary factors that influence the initial ring-back to threshold are the drain–source voltage and the magnitude of the drain current

TABLE II
Empirical Study Model Parameters

Parameter	SiC JFET	SiC MOSFET
L_G	100 nH	520 nH
L_D	300 nH	480 nH
G_{EP}	1.25 mS	1.81 mS
C_2 (near V_{GS}=V_{TH})	900 pF	1.3 nF
C_3	-	700 pF
g_m (near V_{GS}=V_{TH})	10.6-11 mS	5-7 mS
R_{G_NORM}	0.068	0.060
V_{DS} Range	0-400 V	0-400 V
I_D	5.0 A	8.0 A
V_{TH}	-5 V	2.5-4.0 V

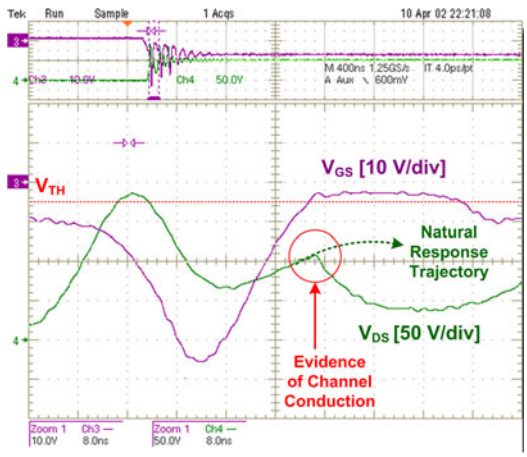

Fig. 14. Establishment of bias conditions for small-signal model during initial cycle of oscillation.

prior to the turn-off event. The drain–source voltage has a nonlinear impact on the establishment of bias conditions, but it has been determined that providing an adequate level of drain current prior to the turn-off event permits the establishment of the proper bias conditions across a wide range of drain–source voltages. An example of the establishment of the proper bias conditions for the SiC JFET test circuit can be seen in Fig. 14. Note that during the initial cycle of oscillation, the gate–source voltage rings back to the device threshold voltage. Time correlated with reaching threshold is the observation of a disturbance in the drain–source voltage. This perturbation in the drain–source voltage is direct evidence of channel conduction and nonzero transconductance, and justifies the bias condition necessary for application of the small signal model. Once this bias condition is established, the small-signal model is valid and can be used to predict whether the oscillatory behavior is likely to continue indefinitely or not.

A. Empirical Results for SiC Lateral-Channel DMOSFET

A summary of the empirical results for the SiC MOSFET test sequence is plotted in histogram format along with the normalized conductance curves determined by simulation in Fig. 15. From this figure, it can be determined that the small signal model provides good quantitative agreement with the empirical

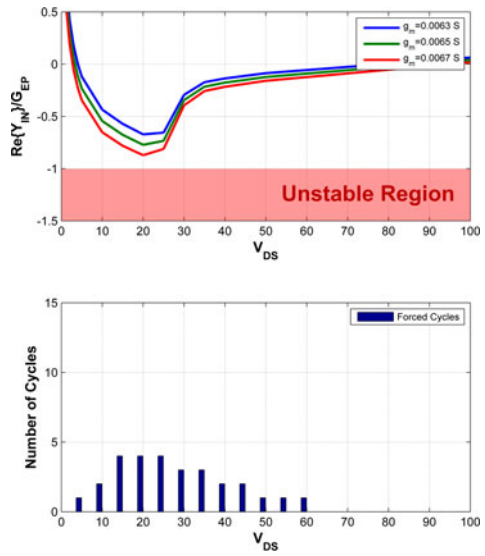

Fig. 15. Empirical results comparison to simulation output for SiC MOSFET.

results based on an envelope of transconductance values that are reasonable for the value of gate–source voltage ring-back observed in these experiments. It is also apparent that the SiC MOSFET does not experience self-sustained oscillation across the envelope of test cases evaluated, but the device does experience a number of forced cycles during the low-voltage region of susceptibility. This behavior is predicted by the model in that the normalized conductance approaches, but does not cross the -1 point. It should also be pointed out that the second region of susceptibility predicted by the model for the SiC MOSFET is also confirmed by experimental evidence in the 30–60 V range. Example time-domain waveforms for SiC MOSFET tests from 10 to 40 V are given in Fig. 16. From this plot it is apparent that the presence of negative conductance distorts the natural response of the drain–source voltage and results in unintended channel conduction in the device. The number of forced cycles present in each of the subplots in this figure corresponds with the histogram summary in Fig. 15. In addition, Fig. 17 presents a comparison of the frequency of forced oscillation predicted by the model and measured in experiment for a range of operating conditions. Note that the natural resonant frequency of the power loop in this test circuit is significantly higher than the frequency of forced oscillation at any operating condition considered. This fact confirms the separation of these two phenomena and corroborates the validity of the analytical model.

B. Empirical Results for SiC Vertical-Channel JFET

A summary of the empirical results for the SiC JFET test sequence is plotted in histogram format along with the normalized conductance curves determined by simulation in Fig. 18. From this figure, it can be determined that the small signal model again provides good quantitative agreement with the empirical results based on an envelope of transconductance values that are reasonable for the value of gate–source voltage ring-back observed in these experiments. It can also be observed from this figure that the SiC JFET-based circuit oscillates in a region of

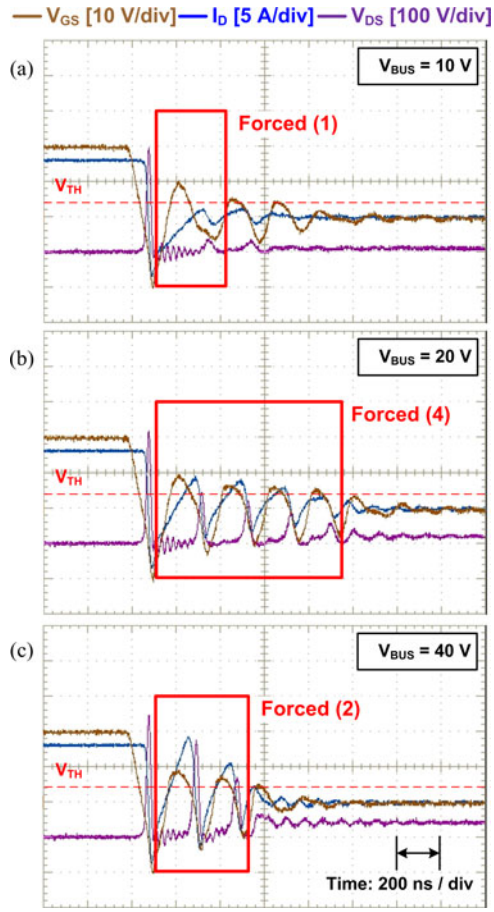

Fig. 16. SiC MOSFET experimental waveforms at several different bus voltage values. One forced cycles is evident at 10 V; four forced cycles are evident at 20 V; and two forced cycles are evident at 40 V.

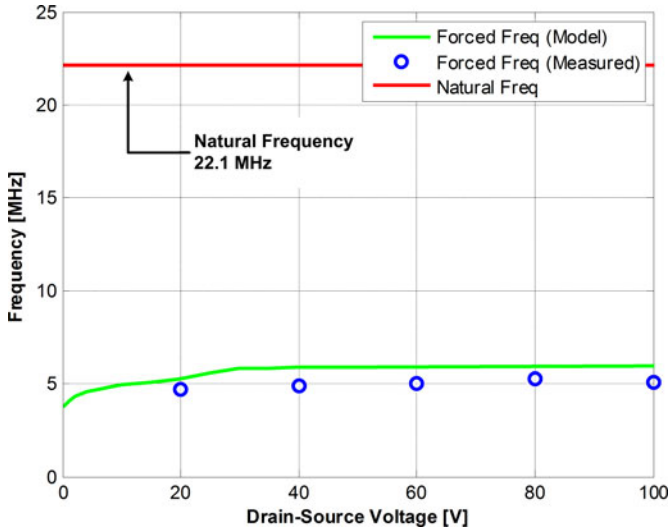

Fig. 17. Comparison of natural and forced frequencies for SiC MOSFET test circuit. The natural resonant frequency of the power loop (upper line) is widely separated from the frequency of forced oscillation predicted by the model (lower line) and measured in experiment (circle markers).

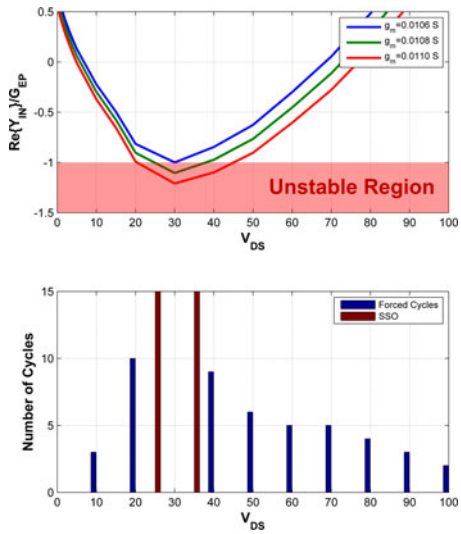

Fig. 18. Empirical results comparison to simulation output for SiC JFET.

susceptibility around 30 V, as predicted by the model. Example time-domain waveforms for SiC JFET tests from 10 to 40 V are given in Fig. 19. From this plot it is apparent that the presence of negative conductance distorts the natural response of the drain–source voltage as a result of unintended channel conduction in the device. The number of forced cycles present in each of the subplots in this figure corresponds with the histogram summary in Fig. 18. In addition, Fig. 20 presents a comparison of the frequency of forced oscillation predicted by the model and measured in experiment for a range of operating conditions. Note that the natural resonant frequency of the power loop in this test circuit is significantly higher than the frequency of forced oscillation at any operating condition considered. This fact confirms the separation of these two phenomena and corroborates the validity of the analytical model.

C. Comparison of SiC MOSFET and SiC JFET Empirical Results

Several instructive inferences can be made based on the results presented in the previous two sections. For example, it can be stated that the lateral-channel SiC MOSFET is generally less susceptible to the occurrence of self-sustained oscillation than the vertical-channel SiC JFET for the range of parasitic values considered. This can be explained in part by the fact that the performance of the SiC MOSFET is farther from ideal SiC unipolar switch behavior when compared to the SiC JFET due to its higher specific on-resistance. As a result of this performance difference, the SiC MOSFET has significantly larger die area, and therefore higher intrinsic capacitances, than the SiC JFET. The larger intrinsic capacitances provide the SiC MOSFET with a substantial self-snubbing capability, which has the effect of reducing its susceptibility to self-sustained oscillation. The SiC MOSFET also switches more slowly than the SiC JFET, which further reduces its susceptibility to self-sustained oscillation. However, as this paper has pointed out, the likelihood of self-sustained oscillation is correlated to switching

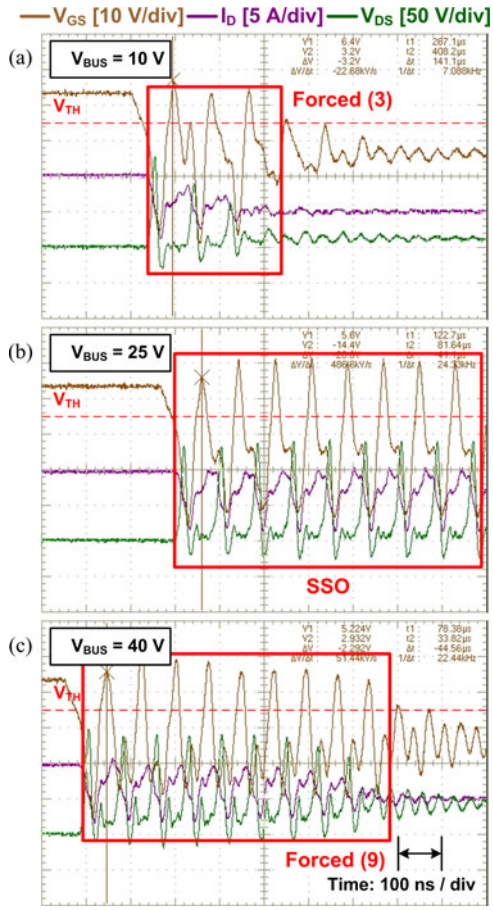

Fig. 19. SiC JFET experimental waveforms at several different bus voltage values. Three forced cycles are evident at 10 V; self-sustained oscillation is evident at 25 V; and nine forced cycles are evident at 40 V.

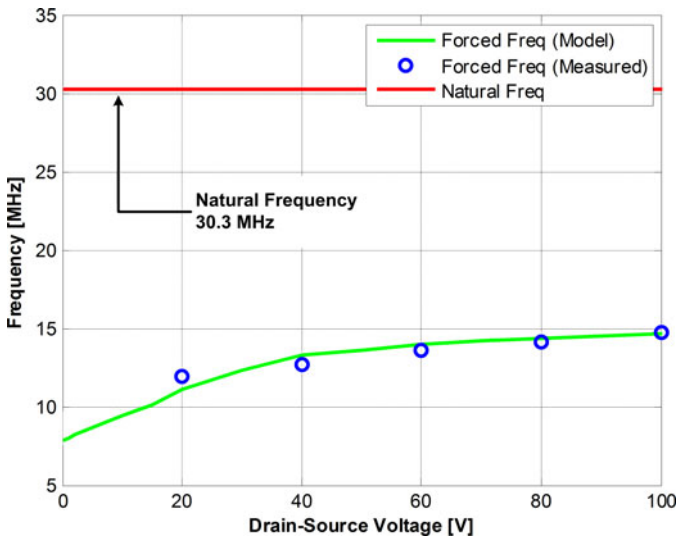

Fig. 20. Comparison of natural and forced frequencies for SiC JFET test circuit. The natural resonant frequency of the power loop (upper line) is widely separated from the frequency of forced oscillation predicted by the model (lower line) and measured in experiment (circle markers).

performance, and therefore advanced device topologies such as the SiC trench MOSFET are more likely to be at risk to self-sustained oscillation. In fact, any device that is capable of switching at high voltage and current slew rates is at risk of experiencing this problem, which explains the prominence of warnings in the GaN device literature. The specific likelihood of occurrence for a given device and circuit can be predicted based on the procedure outlined in this paper, but the general trend evident in the current paper is that higher-speed, lower-capacitance devices are more likely to experience this problem than lower-speed, higher capacitance devices in power electronic circuits designed without this consideration in mind.

VI. Methods for Mitigation of Self-Sustained Oscillation

Several methods are available for reducing the risk of self-sustained oscillation. The most fundamental method is the reduction of stray gate-loop inductance. This should be considered a basic design goal for any application attempting to operate WBG devices at the maximum achievable switching speed. However, since stray inductance cannot be completely eliminated in practical circuits, it may be necessary to augment this strategy, particularly when attempting to maximize the switching speed of WBG devices. The only additional solution in the literature for reducing the risk of self-sustained oscillation is the reduction of switching speed. However, this strategy erodes the benefit of WBG device adoption, and is therefore not an attractive solution for advanced power electronics applications. In the case that the reduction of switching speed is accomplished by increasing the value of the series gate resistance, this solution also increases the risk of Miller turn-on (and shoot-through in half-bridge circuits). Clearly, better techniques are needed to reduce the susceptibility of applications to self-sustained oscillation without trading away the low-loss switching behavior that is one of the major attractions of WBG devices. In the case of the SiC vertical-channel JFET with negligible drain–source capacitance, one effective solution is to add a small ballasting capacitor across the gate–source terminals, close to the die. This additional capacitance has an effect on the conductance curves similar to that observed when the normalized gate resistance is increased as shown in Fig. 10. However, in the case of adding external gate–source capacitance, the stabilizing effect does not depend on the reduction of switching speed, and it has the ancillary benefit of reducing the risk of Miller turn-on. In the case of a device with significant drain–source capacitance such as the SiC DMOSFET, the addition of a ballasting capacitor across the gate–source terminals has a more complex relationship on stability. In this case, the amount of external capacitance required to produce a stabilizing effect is greater than that required for the device with negligible drain–source capacitance. In addition, the stabilizing effect is not universal and small values of external gate–source capacitance may actually produce a de-stabilizing effect. This result also holds true for the vertical-channel JFET when an anti-parallel diode is bonded with the transistor in the package. A quantitative study of these complex influences, along with empirical validation, will be reported in a manuscript in preparation. Another technique being investigated by the authors is the application of closed-loop gate–source voltage control within the gate-drive circuit. The preliminary results of this study have demonstrated a measurable reduction of the risk of self-sustained oscillation due to the feedback action of the controller [44].

VII. Conclusion

WBG field effect transistors have reached a level of maturity that enables their use in practical power electronics applications. However, in order to realize the system-level performance advantages expected form adoption of these devices, application designers must grapple with the implications of operating near-ideal switching elements in practical circuits containing nonnegligible parasitic inductance. One undesirable implication is the possibility of constant-envelope, self-sustained oscillation of the wide bang-gap device(s). This paper has presented an analysis of this phenomenon based on a description of the WBG device and a minimal set of parasitic elements as an unintentional negative conductance oscillator. This methodology is well known in the oscillator design community but has not been previously applied to the oscillation of a power circuit containing wide band-gap devices. The predictive utility of the model presented in the current paper has been validated by an empirical study involving two separate WBG device topologies: the SiC vertical-channel JFET and the SiC lateral-channel MOSFET. The sensitivity of this phenomenon was studied with regard to various device and circuit parameters, and it was found that susceptibility to this phenomenon is increased with reduced gate-loop damping and with increased device transconductance. In addition, it was found that device intrinsic drain–source capacitance provides a self-snubbing function that can influence susceptibility to self-sustained oscillation. Devices with higher specific on-resistance and higher intrinsic capacitances (e.g., SiC MOSFET) are at reduced risk to this phenomenon, whereas devices with lower specific on-resistance and lower intrinsic capacitances (e.g., SiC JFET and GaN HFET) are at increased risk to this phenomenon. This trend suggests that the extent to which a given WBG device approaches the behavior of an ideal switch is the extent to which it is at risk to the phenomenon of self-sustained oscillation. Thus, it is expected that continued maturation of WBG devices will result in increased susceptibility to this problem as the performance of these devices improves. Mitigation of this trend is possible by considering this issue during the detailed design of circuits and power modules, as is universally done in the RF community. The primary contribution of this paper is the identification and empirical validation of an analytical procedure that can be employed by power electronics application designers to enable avoidance of self-sustained oscillation by design, rather than by trial and error.

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