

# Ensuring Volt-Second Balance in High-Power-Density Phase-Shifted Full-Bridge Converter Design

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**Abstract**—The phase-shifted full-bridge (PSFB) converter topology provides a platform which enables the achievement of high power-density through low-loss operation at high frequency. However, this topology is also subject to the risk of flux imbalance in the main power transformer if precautions are not taken to prevent its occurrence. This paper evaluates the power-density implications of the several known mechanisms described in the literature for ensuring flux balance in the context of this converter topology. Additionally, the details of a high-power PSFB prototype converter design are reported and the performance of this system is used to evaluate the practicality of implementing a novel technique for addressing the volt-second balance issue without compromising the converter bus design required to achieve higher power density.

## I. INTRODUCTION

The phase-shifted full-bridge (PSFB) converter is a well-known topology which supports high efficiency operation at high frequencies through the achievement of zero-voltage-switching (ZVS) as described in [1]-[4]. As with any transformer-isolated topology, the achievement of volt-second balance in the power transformer is essential to prevent core saturation and current runaway. In the literature, two primary means for addressing this issue are described. The first is the use of a DC blocking capacitor in series with the transformer primary winding to prevent the flow of DC current [5]; the second is the application of some form of peak-current-mode control (PCMC) [6][7]. The use of a DC blocking capacitor in a high-power converter is undesirable due to the size of the capacitor with the requisite ratings and the creation of an additional failure mode due to the risk of dielectric breakdown of this capacitor during start-up or load-change-induced transients. On the other hand, the use of the PCMC control scheme is also known to be effective at eliminating volt-second imbalance in this topology, and this strategy does not require the use of DC-blocking capacitors. However, the method commonly used to implement this scheme in the PSFB topology is ultimately incompatible with increasing the switching frequency due to the position of the current sensing transducer, which could result in a significant power-density

limitation. In this paper, the factors which underlie this limitation are analyzed, and an alternative solution is proposed which eliminates the power density limitation imposed by the traditional PCMC implementation method.

## II. PSFB CONVERTER OPERATION

Before discussing the power density implications of the current transducer placement, a brief synopsis of the operation of the PSFB converter will be provided.

### A. Synopsis of Operation

The primary-side schematic of the PSFB converter is shown in Fig. 1. The implementation of the rectifier on the secondary side does not dominate the determination of flux balance in the power transformer and can therefore be ignored in the present analysis. The conventional phase-shift modulation (PSM) scheme used in PSFB converters is illustrated in Fig. 2 and the relationship of these switching events to the operation of the PSFB converter is shown in Fig. 3 [1]-[5]. According to this scheme, each of the primary-side switches is operated at a fixed duty cycle of approximately 50%, and the switches in each phase leg are operated in anti-phase with a small dead-time preventing shoot-through. The duty cycle of the converter is determined not by varying the width of on-state intervals as in the case of a hard-switched

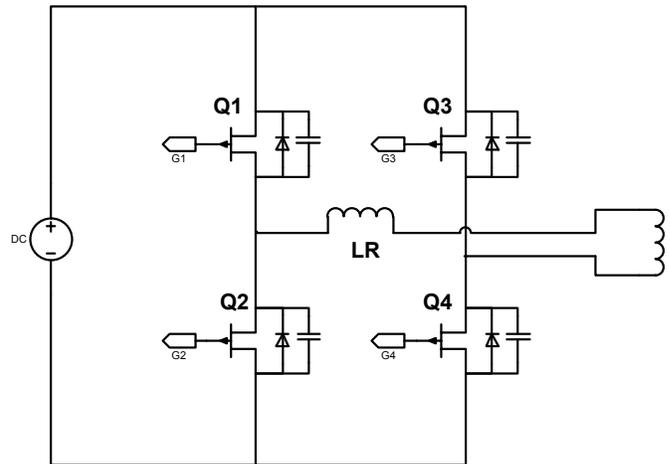


Figure 1: PSFB summary schematic (primary side)

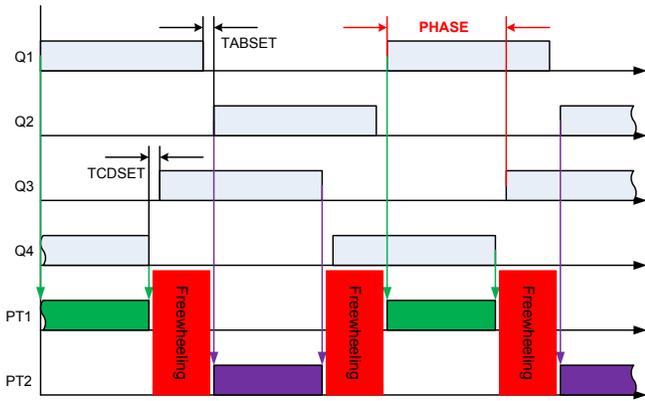


Figure 2: Phase-shifted gating sequence

full-bridge converter, but rather by varying the phase shift between the switches in the two phase-legs. For example, the  $Q_1/Q_2$  leg is shifted with respect to the  $Q_3/Q_4$  leg in order to simultaneously determine the width of the two power transfer intervals shown in the figure, PT1 and PT2. Between the power transfer intervals PT1 and PT2, a freewheeling interval occurs during which there is no power transferred across the transformer. During this freewheeling interval, the primary-side transformer voltage is shorted; in this state either the top two switches ( $Q_1$  and  $Q_3$ ) or the bottom two switches ( $Q_2$  and  $Q_4$ ) are simultaneously conducting. This interval sets up the zero-voltage-switching event because the freewheeling current is utilized to redistribute energy from the output capacitance of the switch which is turning ON (e.g.  $Q_4$  at the end of PT2) to the output capacitance of the switch which is turning OFF (e.g.  $Q_2$  at the beginning of PT1).

### B. Controller Degrees of Freedom

In Fig. 2, it can be seen that there are three control variables available to the PSFB controller: (1) PHASE, which represents the phase shift between  $Q_1/Q_2$  and  $Q_3/Q_4$ ; (2) TABSET, which represents the dead-time between  $Q_1$  and  $Q_2$ ; (3) and TCDSET, which represents the dead-time between  $Q_3$  and  $Q_4$ . The PSFB design literature describes the role that the two dead-time intervals play in ensuring that the active-to-passive and passive-to-active resonant transitions will occur, respectively [1]-[5],[9]. The duration of these two dead-time intervals is typically tuned during converter commissioning in order to maximize the benefit of the resonant transitions described previously. Besides these dead-time intervals, the only remaining degree of freedom available to the PSFB controller is the phase shift between the two converter legs. This phase shift is used as the PSFB control parameter which is regulated in order to provide a constant voltage or current on the converter output. At first glance, it appears that the PSFB converter has an insufficient number of independent control parameters to support the dual requirements of (1) providing a regulated output, and (2) achieving volt-second balance in the power transformer. In other words, since a single control parameter, PHASE, is responsible for determining the duration of both power transfer intervals PT1 and PT2, there is no additional mechanism available for correcting an offset in the primary current which may develop due to dead-time asymmetry, digital controller latency, un-

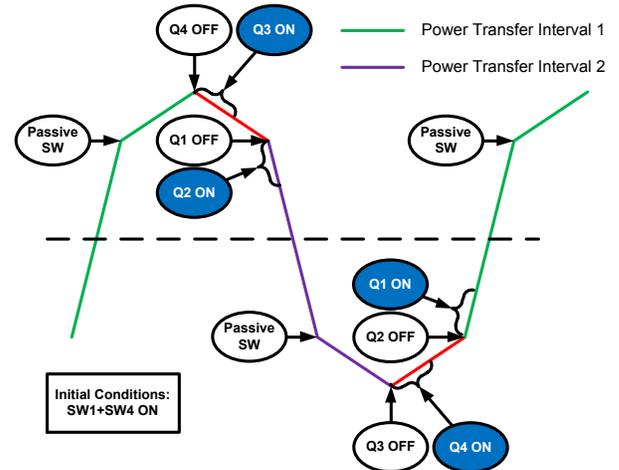


Figure 3: PSFB primary current waveform

matched components, or the like. However, upon further consideration it is observed that a simple extension to the conventional phase-shift modulation technique can be used to resolve this apparent problem. This extension involves updating the PHASE variable twice during each switching period: once to determine the duration of PT1, and once to determine the duration of PT2. This results in an effective second degree of freedom which permits the PSFB controller to regulate the converter output while simultaneously reducing the risk of flux imbalance in the power transformer. This technique is utilized in PSFB implementations which rely on PCMC such as that described in [12].

### III. PSFB DESIGN FOR MAXIMUM POWER DENSITY

One requirement imposed on the design of a PSFB converter operating under PCMC has to do with the implementation of the primary current sensing element. Due to the presence of subtle asymmetries in the PSFB converter, it is possible for the system to develop a DC offset in the primary current waveform. If a current transformer in series with the transformer primary winding is used as the input to a PCMC scheme, this DC current will not be detected by the controller and this configuration will generally lead to transformer saturation [10][13][14]. Several methods are described in the literature for resolving this issue: Stuart recommends the use of a Hall effect sensor in place of the current transformer [13]; Walters and Polivka recommend the use of two separate current transformers in one leg of the converter [14]; and Redl et. al recommend the insertion of a single current transformer in the DC bus between the input capacitor bank and the full-bridge [10]. However, none of these solutions are appropriate for a PSFB converter intended to meet an aggressive power density requirement. Such a design requires operation at high switching frequency ( $> 100$  kHz) in order to reduce the size of the magnetic components. The bandwidth requirement for the current transducer when such a system is operated in PCMC is beyond the capabilities of all but the most expensive hall-effect sensors. The utilization of multiple current transducers likewise has an obvious negative impact on the design of a PSFB converter due to the additional component size and cost. The remaining option, which involves placing the current transducer between the input energy storage and the transistor bridge elements, has a more subtle but similarly deleterious impact on the

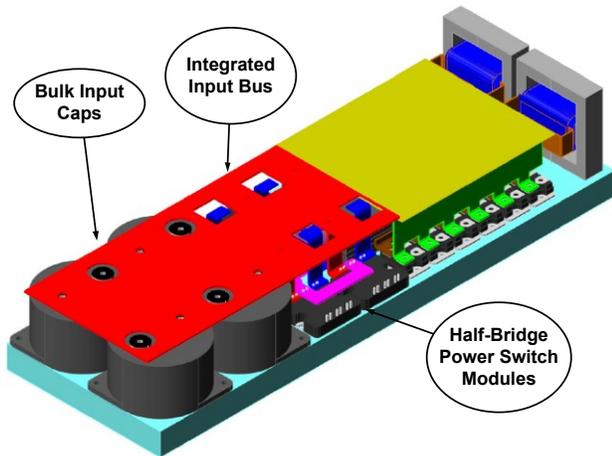


Figure 4: Example high-frequency converter design showing integrated bus structure

performance of a high-power-density PSFB converter. This is because the design of the high-power input bus is critical for enabling high performance and high power density in such a system. The preference is for a wide and flat bus but placing the current transducer in series with the bus can introduce a bottleneck that geometrically restricts high-bandwidth pulsed current flow to a small area. This arrangement increases both the input loop inductance and bus resistance. Such restrictions mitigate the benefits that may be gained from low ESL/ESR input capacitance and reduce the effectiveness interleaved bus structures have in eliminating skin effect issues. Fig. 4 shows an example of a high-power-density PSFB converter design which has an interleaved input bus designed to provide a low-impedance connection between the input energy storage elements and the full-bridge switching elements. Monitoring current at the transformer primary connection, on the other hand, can resolve these challenges. Most transformer primary connections require that current flow be tapered to a narrower point of connection where the inductance, dominated by the transformer primary, is utilized by the PSFB to achieve resonant switching. By sensing current at this interface, the true instantaneous switch current can be measured without increasing bus impedance unnecessarily. Furthermore, measurement at this point is in series with both halves of the bridge transistors thus the loop impedance will be identical for each phase of a switching cycle. It is therefore desirable to provide a mechanism which permits effective utilization of a current transducer placed in series with the transformer primary winding without introducing the risk of transformer saturation nor requiring the use of power density reducing DC blocking capacitors.

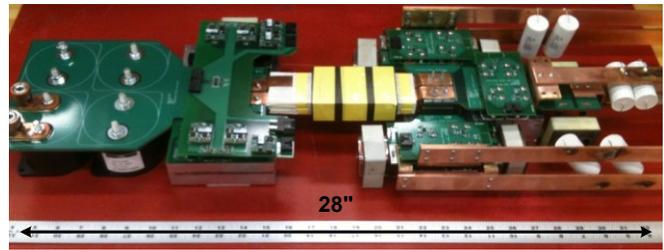


Figure 5: High power-density phase-shifted full-bridge converter prototype

#### IV. EMPIRICAL EVALUATION OF PROTOTYPE CONVERTER

A high-power PSFB converter was designed, constructed, and evaluated as part of this work in order to examine the implications of designing the system for maximum power density. This converter is based on the topology shown in Fig. 1, but utilizes high-performance Silicon Carbide enhancement-mode JFETs for the primary-side switches. A picture of the prototype converter is shown in Fig. 5. During the baseline evaluation of this system, the converter was fitted with a set of blocking capacitors in series with the transformer primary winding in order to prevent the development of a DC current which could lead to transformer saturation. In this configuration, the prototype converter was demonstrated to successfully achieve the designed output power of 30 kW while operating from an input voltage of 550 V. Subsequent to the baseline analysis, further evaluation was carried out without the DC blocking capacitors in order to determine the characteristics of the expected DC offset current in the primary winding as a function of load. An example of the DC offset observed at two load levels (light and heavier) is presented in Fig. 6(a) and 6(b). In these figures, it is observed that the system incurs little DC offset in the primary current at low output power levels. However, at power levels approaching 2 kW, a significant DC offset appears in the primary current. This converter will reach a point at which the transformer saturates, as shown in Fig. 6(c). Therefore, this configuration requires the introduction of additional controller sophistication in order to zero out this offset and prevent transformer saturation. A mechanism capable of providing this additional feature is described in the next section.

#### V. AUGMENTED CONTROLLER SOLUTION

In order to satisfy the most demanding power density requirements, it is desirable to place the current transducer in series with the transformer primary winding, as suggested by the discussion on high-power bus design in the previous section. However, this current transducer placement necessitates an alternate strategy to prevent volt-second imbalance in the transformer.

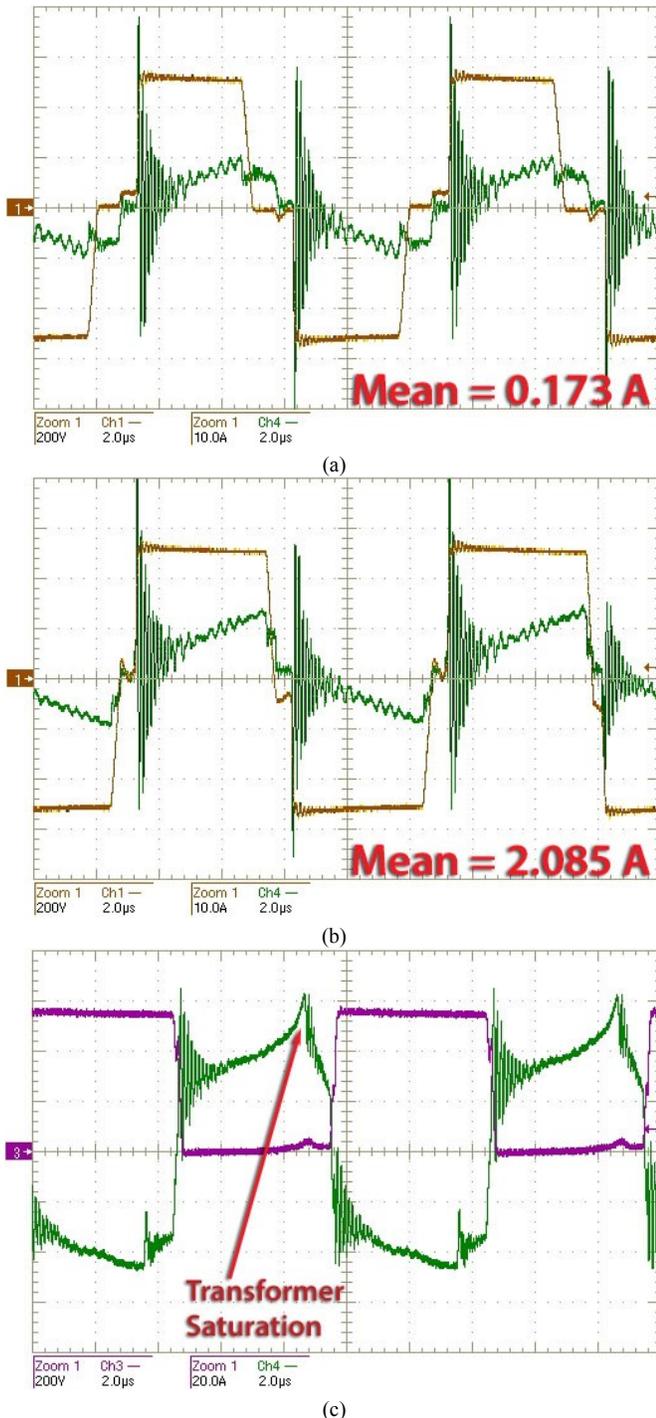


Figure 6: Evidence of imbalanced transformer primary current increasing with load in PSFB converter. (a) Light load operation with near zero current imbalance. (b) Heavier load demonstrating obvious current imbalance. (c) High load operation demonstrating transformer saturation due to current imbalance. Channel 4 (green trace) is the primary current waveform in all sub-plots.

Toward that end, this paper proposes a novel controller solution which introduces an additional degree of freedom into the controller in order to separately manage the current set-point and the transformer volt-second balance. A generalized controller design such as that frequently used in PSFB converters is shown in Fig. 7. In this figure, it can be seen that

the control system incorporates an inner peak-current-mode control loop based on input from a high-bandwidth current transducer such as a current transformer, and an outer voltage control loop based on monitoring the output voltage. This second outer control loop is not strictly necessary for the purpose of managing the volt-second balance in the transformer and will therefore not be given further consideration in this paper. One way in which the inner control loop is frequently implemented is by rectifying the current transducer output and supplying the rectified reference current to a single comparator which serves as the basis for latching the gate signal states for both power transfer intervals. The other input to this comparator is a slope-compensated version of the reference current supplied by the outer control loop. As discussed previously in this paper, this configuration automatically ensures volt-second balance in a system which incorporates the current transducer in the power bus. It should be noted that it is usually necessary to condition the signal from the high-bandwidth current transducer with a low-pass filter in order to prevent false-triggering of the analog comparator due to ringing which results from the natural response of parasitic elements in the power stage.

However, for the case of a system with a current transducer in the desired location, two changes are needed to the traditional PSFB controller design shown in Fig. 7. First, the comparator function in the traditional controller architecture must be separated into two individual components, one of which is applied to each direction of the primary current flow. This separation can be done in several ways. One method is to preserve the full-wave rectified transducer signal and separate the peak current intervals within the controller by recognizing that the two polarities are represented in an interleaved manner in the rectified transducer signal. A simpler approach is to remove the rectifier and to present the bipolar transducer signal to the analog comparator. Accordingly, the comparator logic within the controller is duplicated and the two paths are fed inverted representations of the reference current. A second change which is required to the traditional PSFB controller is the addition of a second current transducer which is capable of detecting the DC current offset which can occur in the transformer primary. A simple example is a shunt current measurement in the same location as the high-bandwidth current sensor. The purpose of this second sensor is to provide the ability for the controller to observe the DC primary current flow and apply a correction to the gate-drive signal before a substantial flux imbalance can develop. This observation of the primary offset current can be supplied to a compensated error amplifier which introduces a corrective output into the current reference in order to drive this error signal to zero. The output of this ancillary control loop is simply added into the two copies of reference signal provided by the outer voltage-control loop in order to remove the DC offset current. An example implementation of this augmented controller design is shown in Fig. 8. In this figure, the additional components which are introduced compared to the standard controller design shown in Fig. 7 are outlined in blue.

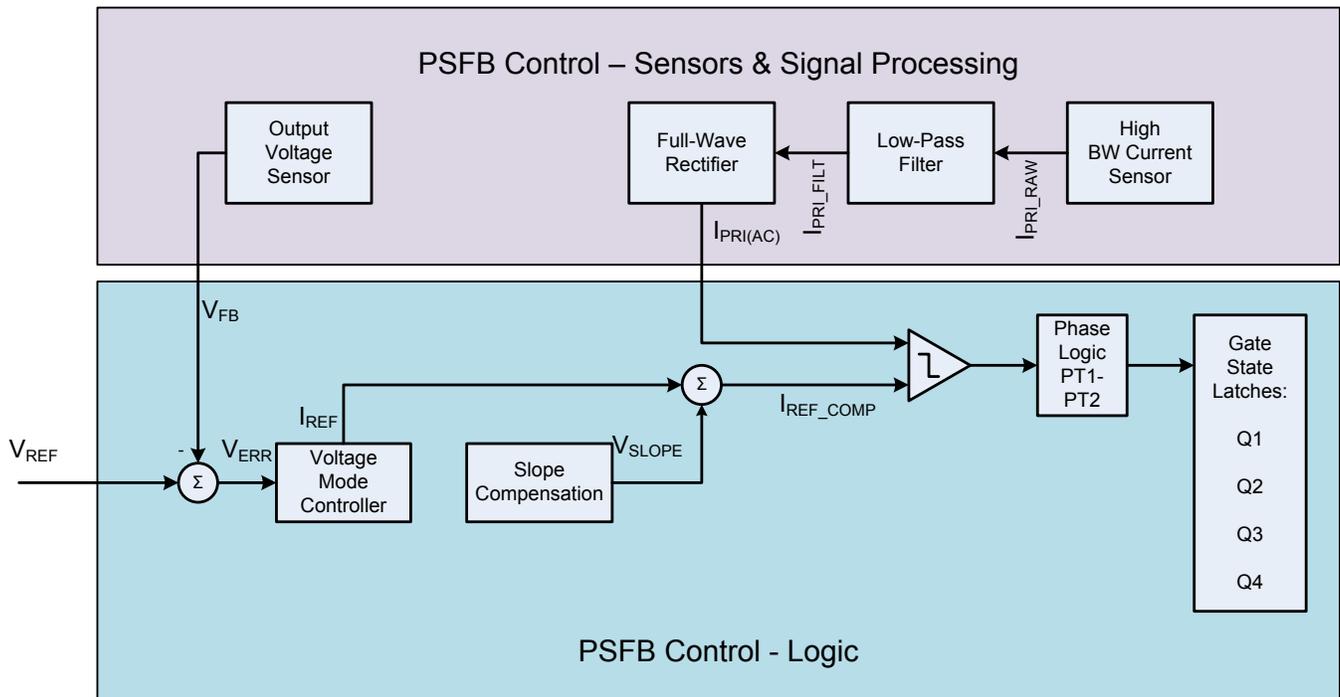


Figure 7: Generalized phase-shifted full-bridge controller diagram

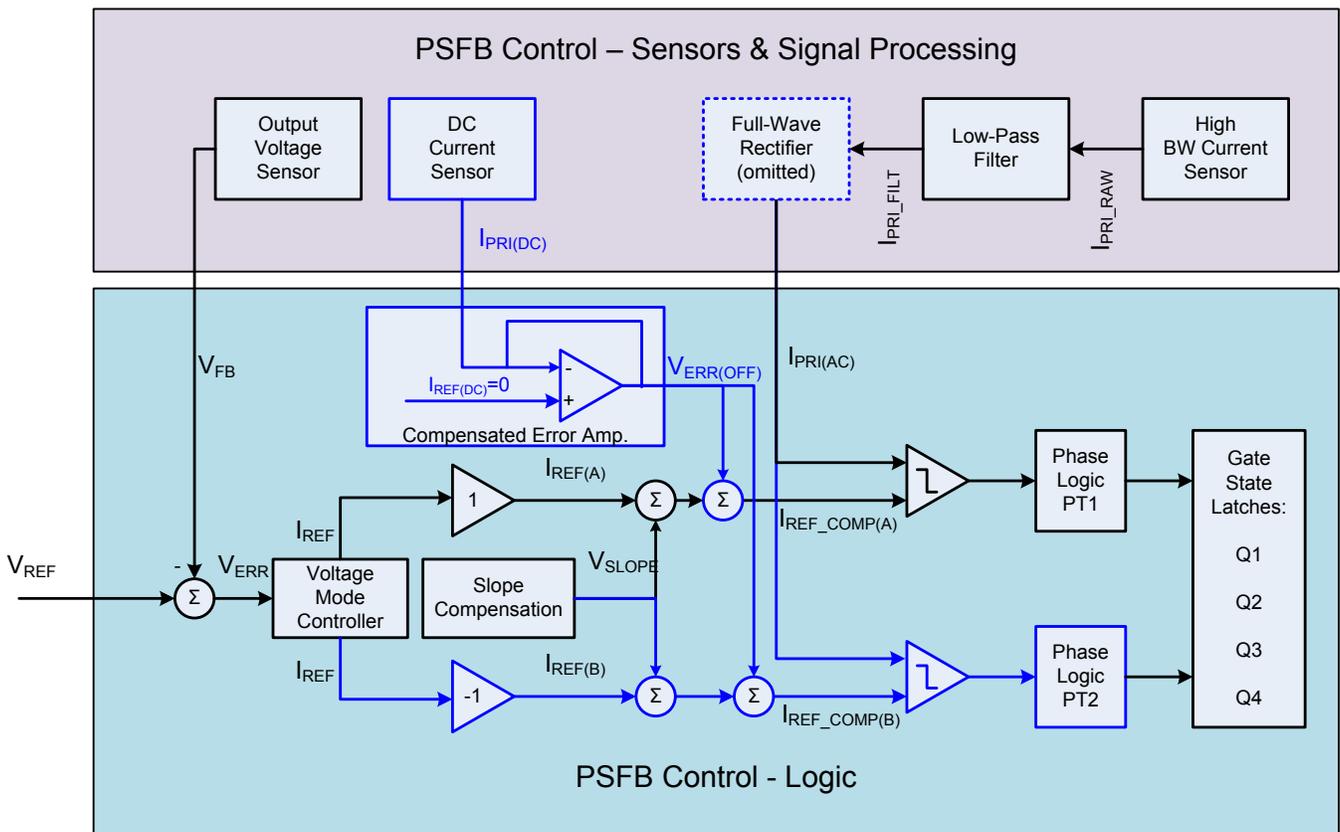


Figure 8: Proposed phase-shifted full-bridge controller diagram

## VI. EVALUATION OF NOVEL CONTROLLER SOLUTION

The control solution proposed in the previous section has been evaluated by means of a full-bandwidth simulation of the high-power PSFB converter example described in the empirical analysis section of this paper. With the proposed control algorithm disabled, this simulation can be observed to exhibit a flux imbalance when a small asymmetry is introduced into the power stage of the converter, for example by increasing the  $R_{DS(ON)}$  of the primary-side switches in only one phase leg of the converter. An example simulation output which demonstrates the effect of such a small asymmetry on the pertinent waveforms of the converter is presented in Fig. 9. It should be noted that there is a measurable DC offset in the primary current waveform shown in this figure of approximately 1.20 A. In this simulation, the DC current transducer is implemented as a 10 m $\Omega$  shunt which is then filtered by a single-pole low-pass filter with a corner frequency of approximately 5 Hz and subsequently amplified to produce a transducer gain of 1 V/A. Fig. 9 demonstrates the operation of the converter after 100 ms, or after approximately 3 times the low-pass filter time-constant value. At this time, the DC signal can be observed to have nearly settled on the value expected for the observed value of primary current offset. It should also be noted that the effect of filtering the high-bandwidth current sensor output is evident in the top subplot of this figure. In this simulation, a single-pole low-pass filter with a corner frequency of approximately 1 MHz is utilized. This filter design was selected in order avoid empirically observed false-triggering in the converter

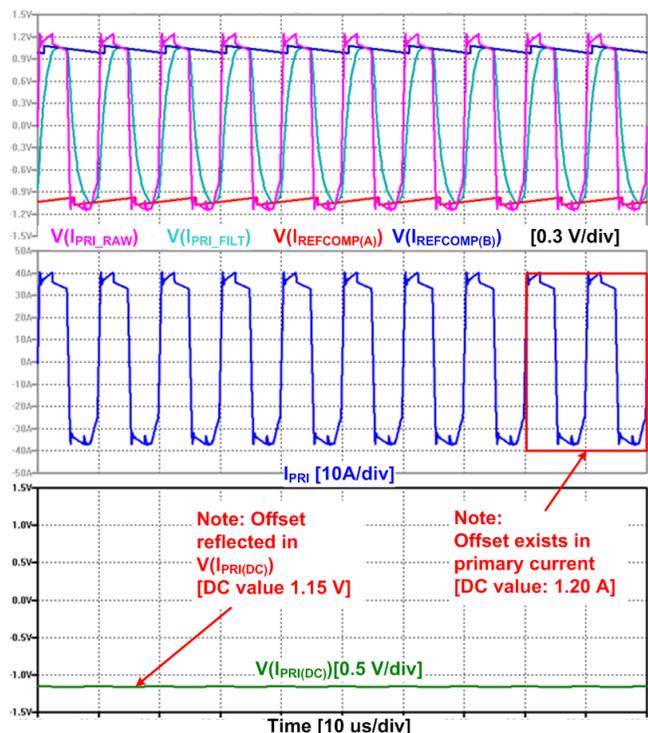


Figure 9: Simulation output demonstrating DC offset resulting from power stage imbalance in PSFB converter without the updated control algorithm; the top subplot shows the primary current AC transducer output along with the slope-compensated reference signals; the middle subplot shows the primary current waveform; the bottom subplot shows the primary current DC transducer output filtered with a single-pole low-pass filter. The signal labels correspond to the signal names shown in Fig. 7.

prototype demonstrated in Fig. 5. One important side-effect of filtering the high-bandwidth current transducer signal is that the comparator output is delayed with respect to the crossing of the non-filtered primary current signal and the reference current waveform. This latency introduces the possibility of primary current runaway because the rapidly increasing di/dt which results when the transformer approaches saturation is adequate to result in the development of a destructive current level during this delay. This mechanism is the root cause of loss of control of the peak current shown in Fig. 6(c) despite the use of peak-current-mode control.

A second simulation result demonstrating the effect of the proposed control algorithm is shown in Fig. 10. In this example, the same power-stage asymmetry used in the previous example is present in this configuration of the simulated PSFB controller. In addition, the influence of the proposed controller algorithm has been enabled by adding the compensated error amplifier output to the reference current signals. As a result, the flux imbalance which was present in the previous example is driven to an acceptably negligible level by the action of the error amplifier. This effect can be observed both in the DC value of the primary current signal, as well as in the value of the DC current transducer output.

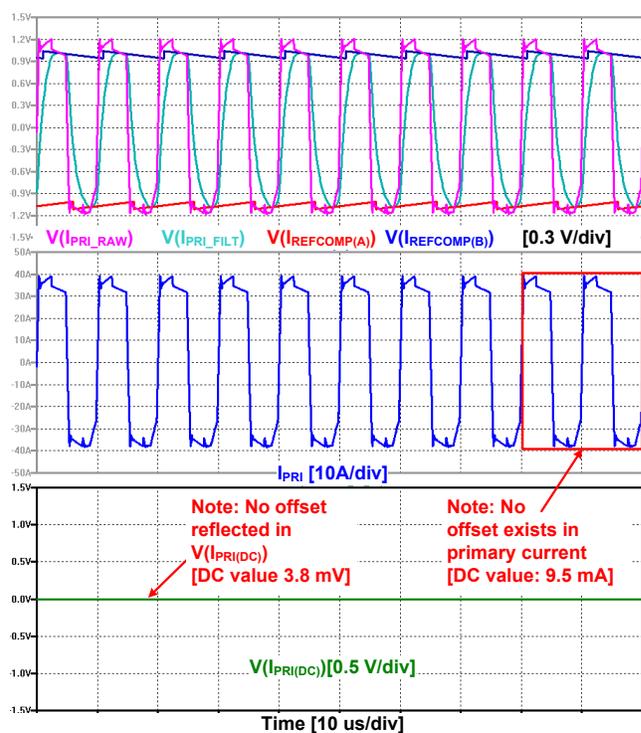


Figure 10: Simulation output demonstrating elimination of DC offset by introduction of the proposed PSFB control algorithm; the top subplot shows the primary current AC transducer output along with the slope-compensated reference signals; the middle subplot shows the primary current waveform; the bottom subplot shows the primary current DC transducer output filtered with a single-pole low-pass filter. The signal labels correspond to the signal names shown in Fig. 8.

## VII. CONCLUSION

The requirement to manage the flux balance in the power transformer of a PSFB converter is a critical part of the design process which has received extensive treatment in the literature. However, much of the available literature has ignored the power-density implications of utilizing the conventional techniques for ensuring this requirement is met in the context of the PSFB topology. This paper evaluates the implications of implementing peak-current-mode control with a current transformer in the primary path of the transformer which is known to leave a risk of saturable volt-second imbalance in the power transformer. But this placement is also advantageous in the sense of designing an efficient converter that operates at high switching frequency and thus enabling an increase in power density. The problem of volt-second imbalance is shown to be resolved by use of asymmetric phase shift as an independent degree of freedom that is controlled by a low-bandwidth control loop introduced into the peak-current reference. Successful operation of the prototype converter built as part of this work demonstrates that the expected primary current offset which results from this design decision is readily observable. The augmented controller will be validated in a future paper reporting the experimental result of using the dual-sensor control scheme described here. It is expected that this control solution will achieve transformer flux-balance while simultaneously providing a power-density advantage over the likely alternatives.

## REFERENCES

- [1] B. Andreyca, "Designing a Phase-Shifted ZVT Power Converter." Unitrode Corp., Merrimack, NH, Mar. 1993.
- [2] B. Andreyca, "Design Review: 500 Watt, 40W/in<sup>3</sup> Phase Shifted ZVT Power Converter." Unitrode Corp., Merrimack, NH, Mar. 1993.
- [3] O. D. Patterson and D. M. Divan, "Pseudo-resonant full bridge DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 6, no. 4, pp. 671–678, 1991.
- [4] R. Ayyanar and N. Mohan, "Zero Voltage Switching DC-DC Converter," U.S. Patent 6,310,785, Oct. 2001.
- [5] N. H. Kutkut, "A full bridge soft switched telecom power supply with a current doubler rectifier," in *Proc. Power and Energy Systems in Converging Markets*, 1997, pp. 344–351.
- [6] S. Han, I. Munuswamy, and D. Divan, "Preventing Transformer Saturation in Bi-Directional Dual Active Bridge Buck-Boost DC / DC Converters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 1450–1457.
- [7] H. R. Weischedel and G. R. Westerman, "A Symmetry Correcting Pulsewidth Modulator for Power Conditioning Applications," *IEEE Transactions on Industry Applications*, vol. IA-9, no. 3, pp. 318–322, May 1973.
- [8] D. Costinett, D. Seltzer, D. Maksimovic, E. D. Costinett, and R. Zane, "Inherent Volt-Second Balancing of Magnetic Devices in Zero-Voltage Switched Power Converters," in *Proc. Applied Power Electronics Conference (APEC)*, 2013, pp. 9–15.
- [9] "Green Phase-Shifted Full-Bridge Controller with Synchronous Rectification," Texas Instruments Inc., Dallas, TX, Oct. 2011.
- [10] R. Redl and L. Balogh, "A Novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Considerations, and Experimental Results at 1.5 kW, 100kHz," *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 408–418, 1991.
- [11] M. Brunoro and J. L. F. Vieira, "A high-performance ZVS full-bridge DC-DC 0-50-V/0-10-A power supply with phase-shift control," *IEEE Transactions on Power Electronics*, vol. 14, no. 3, pp. 495–505, May 1999.
- [12] "Phase Shifted Full Bridge: CCS User Guide," Texas Instruments, Inc., Dallas, TX, Version 1.1, Mar. 2012.
- [13] T. A. Stuart, "A STUDY OF TWO CONTROL METHODS FOR FULL BRIDGE CONVERTERS." Air Force Systems Command Report #AD-A227, Jun. 1990.
- [14] M. Walters and W. Polivka, "A High-Density Modular Power Processor for Distributed Military Power Systems," in *Proc. Applied Power Electronics Conference (APEC)*, 1989, pp. 403–412.