Letters

Stability Considerations for Silicon Carbide Field-Effect Transistors

Andrew Lemmon, Michael Mazzola, James Gafford, and Chris Parker

***Abstract*—Owing to their very low intrinsic capacitance and on-resistance, silicon carbide FETs have been shown to produce poor dynamics in certain power electronics applications, particularly those based on the half-bridge configuration. This letter catalogs three separate phenomena that are observed in the context of such applications and provides a detailed treatment of the most troublesome of these behaviors: the occurrence of sustained oscillation at switch turn-off. This behavior is analyzed in the context of established oscillator design theory; both simulation and experimental results are shown to verify this analysis; and practical suggestions are made to application designers to manage this behavior.**

***Index Terms*—FETs, oscillation, resonance, shoot-through, silicon carbide.**

I. Introduction

THE recent introduction of commercially available silicon carbide FETs has resulted in a growing movement on the part of application engineers to integrate these devices into commercial power electronics systems. Applications such as solar inverters and traction motor drives, which have until now been the domain of the silicon MOSFET and the silicon IGBT, are now beginning to test the performance claims of SiC, including reduced switching losses, reduced conduction losses, increased efficiency, and reduced thermal management requirements. In some cases, the achievement of these advantages has been accompanied by an increase in undesirable phenomena such as the excitement of new oscillatory modes in the system. One reason why this can happen is that current-generation SiC field-effect devices are characterized by specific on-resistance far lower than high-voltage silicon MOSFETs and do not exhibit tail current at turn-off like silicon insulated-gate bipolar transistors (IGBTs). These characteristics are desirable in the sense that they lead to an expanded design space where reduced conduction and switching losses, are available at high voltage, but they may also result in a lower effective damping ratio for the power loop of the system. Therefore, resonant modes that have been implicitly damped by MOSFET on-resistance or implicitly snubbed by IGBT tail current may become observable in a SiC-based design. Another reason that new oscillatory modes may appear in SiC-based designs is that these devices have lower overall intrinsic capacitance than the competing silicon technologies. As a result, these devices switch very quickly, which in a half-bridge circuit, as shown in Fig. 1, can 1) excite resonances in parasitic elements in the circuit which are reflected as damped oscillations, and 2) create unintended switching events due to the modulation of channel potential caused by charge transported through the gate as displacement current. An example of the former problem (damped oscillations) is illustrated in the turn-off waveform of Fig. 2. This result was obtained by clamped-inductive-load switching of a high-current half-bridge

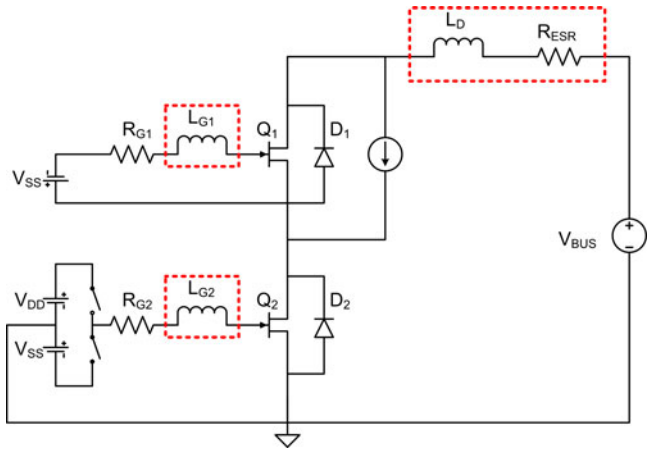

Fig. 1. CIL test circuit used to generate waveforms of Figs. 2–4. Parasitic elements are outlined with red-dashed boxes. Note that the top switch is not actively gated, but is biased OFF. The clamped inductor is represented as a current source.

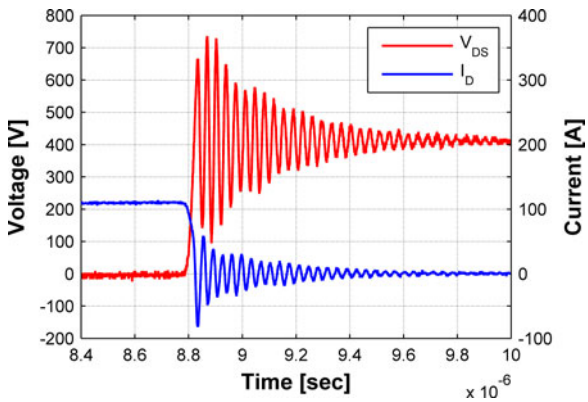

Fig. 2. Half-bridge turn-off showing natural ring-down.

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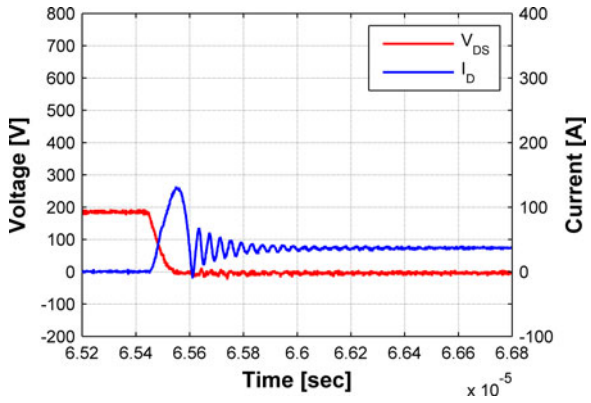

Fig. 3. Half-bridge turn-on showing shoot-through.

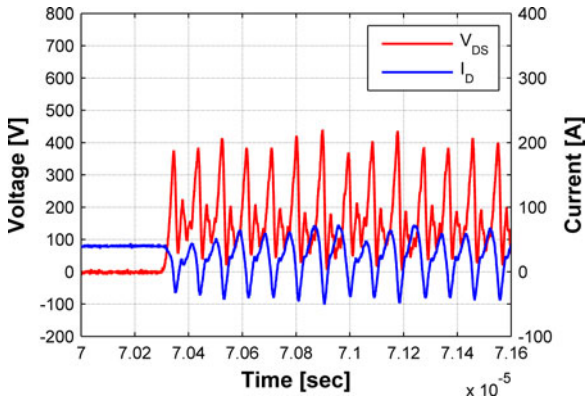

Fig. 4. Half-bridge turn-off showing sustained oscillation.

SiC JFET module, as illustrated by the circuit in Fig. 1. The traditional method for managing oscillations of this sort is by means of an *RC* snubber across the high voltage bus in close physical proximity to the half-bridge, although alternative methods including placing a ferrite bead in the power path have been proposed [2]. Since this phenomenon has been studied in [1]–[3], [9], and [14], and similar experimental waveforms are observed in several papers describing SiC [6]–[8], [10]–[13] and GaN [17] device switching performance, it will not be examined further here. The latter problem, which is typically characterized as "shoot-through," is shown by experimental example in Fig. 3. This phenomenon occurs when the inactive switch in a half-bridge configuration experiences a rapid, positive *dV/dt* event across the drain–source terminals during the time that the active switch drain voltage collapses, resulting in a positive displacement current through the Miller capacitor equal to *C·dV/dt*. If the gate-drive attached to the inactive switch cannot fully sink this displacement current, the intrinsic gate–source capacitor will be charged by the balance of the displacement current and the inactive switch may turn ON. Since this phenomenon has been studied in [4] and [5], it will not be further investigated here.

Another effect observed by the authors which has not been fully described in the SiC power device literature is the phenomenon of self-sustained oscillations at turn-off of the lower switch in the half-bridge configuration. This problem is distinct from both the underdamped natural response and the occurrence of shoot-through, and it can result in destabilizing of the application circuit and even destruction of the semiconductor devices under certain conditions. An extreme example of a post-turn-off sustained oscillation is shown in Fig. 4; in this case, the oscillation continues until the bus voltage source is depleted of energy, or the switch is actively gated on, or failure of the oscillating switch occurs. Another manifestation of this problem is the occurrence of a burst of "forced" oscillations at the end of the switching transition which then damp out like the unforced natural response. Collectively, these behaviors represent the known propensity for instability of half-bridge circuits, although in the authors' experience, this behavior is more likely to occur with devices closer to the SiC unipolar limit than the Si unipolar limit due to the much lower parasitic capacitances.

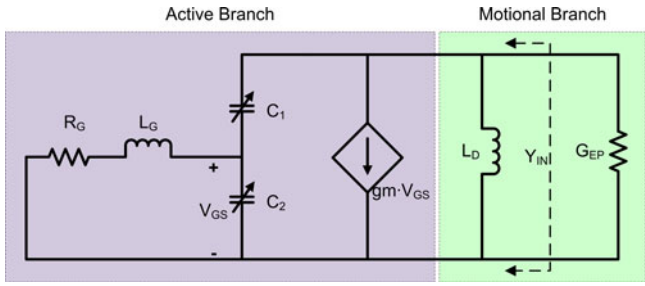

Fig. 5. Small-signal model of power FET oscillator, where $G_{\mathrm{EP}} = [R_{\mathrm{ESR}}[(\omega L_D/R_{\mathrm{ESR}})^2 + 1]]^{-1}$.

The purpose of this letter is to offer a theoretical treatment to understand this issue in the context of existing stability theory and to deduce practical engineering responses for the design of circuits, and especially power modules, containing wide bandgap power semiconductor devices. Section II presents a detailed theoretical treatment of this phenomenon; Section III presents the experimental validation of the theoretical treatment; Section IV presents a set of practical implications for application designers; and Section V concludes this letter.

II. Theory

In contrast to the occurrence of a damped natural response, the phenomenon of forced oscillations cannot be attributed solely to the exchange of energy between parasitic elements. The self-sustaining nature of the oscillations shown in Fig. 4 implies that the energy dissipated by parasitic resistance in the circuit during each oscillation is replaced by a feedback mechanism. An established conceptual framework for describing this process common in the oscillator design community is the negative resistance model [15], [16]. According to this model, a two-leg oscillator can be viewed as a single-port network consisting of an "active" branch and a "motional" branch. For example, the physical circuit shown in Fig. 1 can be abstracted into the small-signal negative resistance oscillator model shown in Fig. 5 by killing independent voltage and current sources and reflecting the power loop parasitic components L_D and R_{ESR} as parallel equivalents, assuming that $\omega L_D \gg R_{\mathrm{ESR}}$. In the case of the high-side switch, the antiparallel rectifier clamps the current source following turn-off of the low-side switch and thus is

a short circuit in the small-signal model. The well-known Barkhausen Criterion states that for any feedback system to attain stable oscillation, the loop gain must equal unity, and the phase delay of the feedback loop must be an integer multiple of 2π rad. Applied to a notional two-branch oscillator, this criterion implies that 1) the conductance in the motional branch must be canceled by a negative conductance in the active branch, and 2) the susceptance in the motional branch must be canceled by an opposite-signed, and equal-magnitude, susceptance in the active branch. In the oscillator design literature, small-signal models are commonly used to predict the stability of sustained oscillation at a given operating point by evaluating these two criteria [16], [18]. Such a small-signal model can be readily constructed to represent an unintentional oscillator composed of a field-effect power transistor with its gate-drive as the active branch, and the associated high-power bus as the motional branch (see Fig. 5).

This model can be used to determine the conditions for sustained oscillation by considering the admittance $Y_{\rm IN}$. From the preceding discussion, it can be observed that the occurrence of sustained oscillation requires that the real part of $Y_{\rm IN}$ be equal to $-G_{\rm EP}$ (first condition), and that the imaginary part of $Y_{\rm IN}$ be equal to zero (second condition). For the special case in which there is negligible gate resistance, $Y_{\rm IN}$ is found to be

$$Y_{\rm IN}(j\omega) = \frac{g_m \frac{L_G}{C_2}}{\frac{L_G}{C_1} + \frac{L_G}{C_2} - \frac{1}{\omega^2 C_1 C_2}} - j\frac{\left(\frac{L_G}{C_1} + \frac{L_G}{C_2} - \frac{1}{\omega^2 C_1 C_2} + \frac{L_D}{C_2} - \omega^2 L_D L_G\right)}{\omega L_D \left(\frac{L_G}{C_1} + \frac{L_G}{C_2} - \frac{1}{\omega^2 C_1 C_2}\right)}. \tag{1}$$

If $G_{\rm EP}$ is assumed to be small, satisfying the first condition can be simplified to the condition that $\mathrm{Re}\{Y_{\rm IN}\} < 0$ which is satisfied by the following inequality:

$$\frac{1}{\omega^2 L_G C_1} > 1 + \left(\frac{C_2}{C_1}\right). \tag{2}$$

This equation must be satisfied at the resonant frequency of the circuit, which is determined by the second condition. Setting the imaginary part of $Y_{\rm IN}$ equal to zero results in the following quadratic equation in ω^2:

$$\omega^4 L_D L_G - \omega^2 \left[\frac{L_G}{C_1} + \frac{L_G}{C_2} + \frac{L_D}{C_2}\right] + \frac{1}{C_1 C_2} = 0. \tag{3}$$

The following procedure can be used to determine the susceptibility of the circuit to sustained oscillation with a given set of component values. First, the quadratic equation (3) is solved for ω, the frequency at which the parasitic drain inductance L_D resonates with the combination of C_1, C_2, and L_G. There are two solutions to this quadratic, and both are valid resonant frequencies of this circuit. However, it can be shown that the higher frequency solution makes $\mathrm{Re}\{Y_{\rm IN}\} > 0$, due to the fact that the left side of (2) is reduced. Therefore, the smaller of the two solutions is the frequency of most relevance for determining susceptibility to sustained oscillation. Next, the calculated resonant frequency is substituted into the real part of (1) to determine whether there is sufficient negative conductance to permit sustained oscillation at this frequency. Carrying out this procedure reveals the fact that for this special case the conductance of $Y_{\rm IN}$ is always negative, which guarantees sustained oscillation provided that $G_{\rm EP}$ is sufficiently small. The more general case, which does not impose the requirement of negligible gate resistance, results in the following expression for $Y_{\rm IN}$:

$$Y_{\rm IN}(j\omega) = \frac{\frac{X_2 + Z_G}{X_2 Z_G} + g_m}{\frac{X_1(X_2 + Z_G)}{X_2 Z_G} + 1} + \frac{1}{X_D} \tag{4}$$

where $X_1 = 1/j\omega C_1$; $X_2 = 1/j\omega C_2$; $Z_G = R_G + j\omega L_G$; and $X_D = j\omega L_D$. Analysis of (4) for the second stability condition demonstrates a result which is cubic rather than quadratic. In this case, reasonable component values can be found which produce both positive and negative conductance for $Y_{\rm IN}$. Therefore, a more detailed treatment of this general case is warranted, especially in light of the nonlinearity inherent in the FET gate-drain or Miller capacitance (represented by C_1). In this letter, (4) was evaluated numerically against the set of parameter values shown in Table I, which were selected to correspond to the empirical evaluation discussed later. The gate resistance is represented as a unit-less quantity $R_{G\_\rm NORM}$ normalized by the characteristic impedance of the gate loop: $R_{G\_\rm NORM} = R_G/[\sqrt{L_G/C_2}] = 2\zeta$, where ζ is the damping ratio of the gate loop. Parameters g_m and C_2/C_1 were evaluated across a range of values because these are nonconstant values in the circuit; parameter $R_{G\_\rm NORM}$ was evaluated across a range of values because it represents the most important degree of freedom in the circuit.

TABLE I
PARAMETER VALUES FOR SIMULATION STUDY

Parameter	Value
L_G	100 nH
L_D	300 nH
G_{EP}	1.25 mS
C_2	900 pF
g_m	7.5-12.5 mS
R_{G_NORM}	0.033-0.100
C_2/C_1 Ratio	0-15

Examples of the outcomes from the simulation study are shown in Figs. 6 and 7. In both plots, the ordinate values represent the real part of $Y_{\rm IN}$ (i.e., the conductance) normalized by the power loop conductance $G_{\rm EP}$. Thus, at a particular operating point, sustained oscillation occurs at –1 on the ordinate. At less than –1, growing oscillations are predicted. It can be observed from these figures that the FET transconductance, the selected gate resistance, and the capacitance ratio C_2/C_1 all strongly influence the susceptibility to oscillation. It can also be inferred that the susceptibility to this phenomenon increases with either increased transconductance or decreased gate resistance. The dependence on the capacitance ratio C_2/C_1 is more difficult to predict, since these curves indicate a "region" of susceptibility at a limited range of C_2/C_1 values. Since the Miller capacitance

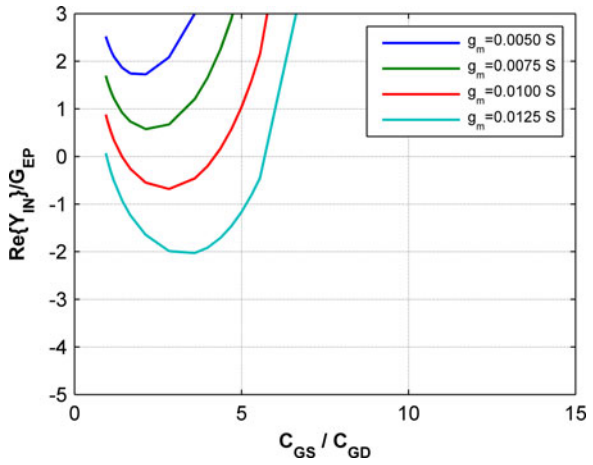

Fig. 6. Conductance of $Y_{\rm IN}$ with $R_{G\_{\rm NORM}} = 0.068$; the parameter is FET transconductance.

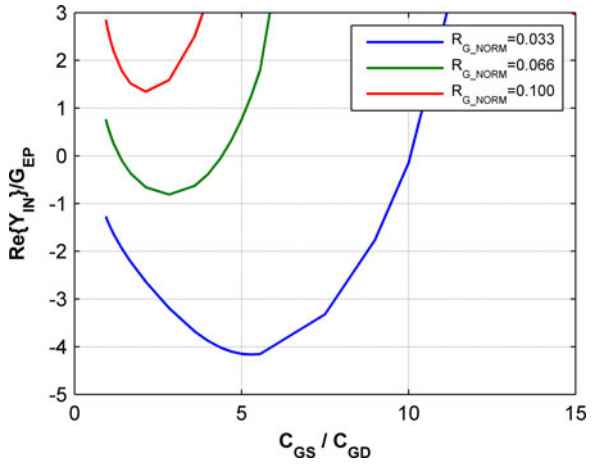

Fig. 7. Conductance of $Y_{\rm IN}$ with $g_m = 10$ mS; the parameter is normalized gate resistance $R_{G\_{\rm NORM}}$.

for a semiconductor device varies nonlinearly with the bus voltage, this theory further predicts risk of sustained oscillation in a specific range of bus voltage, the boundaries of which are dependent on the capacitance of the FET in question.

The validity of this small-signal model depends on several assumptions. First, it is assumed that the transistor transconductance g_m and the gate–source capacitor C_2 can both be linearized about a particular value of $V_{\rm GS}$. Second, it is assumed that the FET Miller capacitor C_1 can be linearized about a particular drain–source voltage. Third, in order for the active oscillator branch to supply negative conductance, it is necessary that the transistor transconductance g_m be nonzero. This implies that the transistor is biased in a way that allows the channel to conduct. In a traditional (intentional) oscillator circuit, a bias network is used in order to satisfy this requirement. In the case of the unintentional power-FET oscillator, this biasing occurs as a result of a parasitic-induced ring-back of the gate voltage, which results in the gate–source voltage being driven to the threshold voltage.

An analytical treatment of this separate but necessary phenomenon will be explored in a separate paper. Here, we provide a qualitative description that will be observable in the experimental results. The operative parasitic component is the gate inductance. During the *dV/dt* event, which in a half-bridge is imposed on the active switch while turning OFF, or on the inactive switch while the active switch is turning ON, displacement current flows through the Miller capacitance and is commutated with negative polarity through the discharge path of the gate drive that includes the parasitic gate inductance. Because energy is stored in this gate inductance, the negative gate current continues while volt–seconds are removed by the negative swing of the gate–source voltage below that of the low-line potential of the gate drive. Thus, the gate inductance and the gate–source capacitance form a series resonant tank that swings the gate–source voltage first more negative than low line, and then more positive than low line. If this positive swing reaches the threshold voltage of the FET, channel conduction may occur which creates an additional current path represented by the dependent current source in Fig. 5. If ring-back falls short of the threshold voltage, then sustained oscillation is not possible. If ring-back to threshold occurs, then the resulting channel conduction will distort the natural response of the two-mesh circuit such that at least one more cycle of oscillation will have the characteristic of being "forced." Ring-back to threshold also enables the bias condition that justifies the small-signal model as a useful tool for determining whether sustained oscillation is likely. Characterizing oscillations as "natural" or "forced" is an important metric used in the following section.

III. Experimental Results

As part of this work, an empirical study was performed to test the theoretical treatment in the previous section. A clamped-inductive-load test stand was utilized for this purpose, with a SJDP120R045 depletion-mode SiC JFET from SemiSouth as the active element. The effective gate resistance R_G was determined to be 0.715 Ω the effective power loop conductance $G_{\rm EP}$ was determined to be 1.25 mS by direct observation of the damping ratio; the C_2/C_1 ratio was swept by varying the bus voltage $V_{\rm BUS}$ from 0 to 400 V; and a constant drain current of 5 A was used for all experiments. Small coils of wire were used to construct L_D and L_G, which were characterized using a Wayne–Kerr precision magnetics analyzer and a custom test fixture suitable for the low inductance involved. The values used for L_D and L_G were 300 and 100 nH, respectively; these values were selected to dominate over the stray inductance on the test board but are not unrealistic levels found in many applications [19].

The first step in the experimental work was to ensure that the required conditions for applying the small-signal model were met. This basically involved creating the ring-back condition to threshold described above so as to bias the transistor to a nonzero value of g_m. It was determined through experiment that the criterion for establishing this bias point is defined by the conditions at the end of the turn-off event, which can be viewed as the initial conditions for the oscillation phenomenon. If the onset of sustained oscillation is to occur, there must be sufficient energy stored in the gate-loop parasitics to allow $V_{\rm GS}$ to ring-back to threshold after the driven portion of the turn-off event

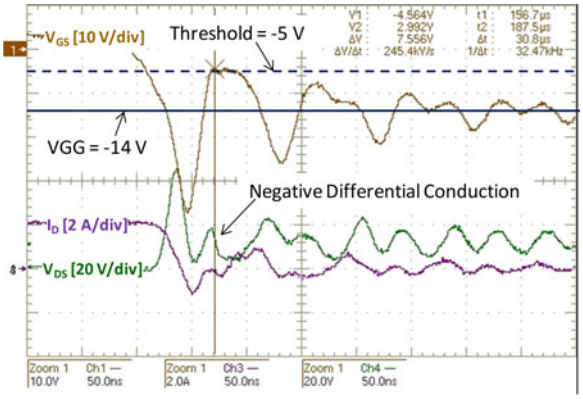

Fig. 8. One cycle of forced oscillation at $V_{\mathrm{BUS}} = 10$ V.

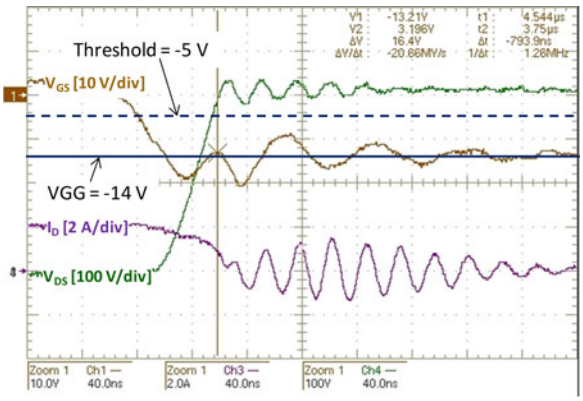

Fig. 9. No forced oscillation at $V_{\mathrm{BUS}} = 400$ V.

(i.e., the period of changing drain–source voltage) concludes. Fig. 8 illustrates this entry-level behavior. Time correlated with reaching threshold is the observation of a disturbance in the drain–source voltage labeled as "negative differential conduction" (NDC) in the figure. The observation of NDC in Fig. 8 is direct evidence of channel conduction and nonzero transconductance and justifies the heuristic method of identifying NDC behavior in the small-signal model. Unless ring-back and NDC occur on the first cycle, only an unforced natural response will occur. An example of this is seen in Fig. 9 where the conditions are not favorable for the first oscillation, and nothing but an unforced natural oscillation results. It can be concluded that the conditions for which the first forced oscillation can occur are highly relevant to the creation of practical engineering responses to prevent the occurrence of sustained oscillation. In this case, a counterintuitive situation is revealed. At the very low bus voltage of 10 V (see Fig. 8), the condition is observed to exist. At the much higher bus voltage of 400 V (see Fig. 9), the condition does not exist primarily because of the nonlinearity of the Miller capacitance. However, the condition for first oscillation can exist at higher bus voltage. The properties of the initial oscillation and the NDC that follows were found to be sensitive to the values of gate-loop inductance L_G and resistance R_G for the obvious reason that along with the gate–source capacitance, these parasitics define the natural response of the gate loop. But the phenomenon is also sensitive to the magnitude of the drain

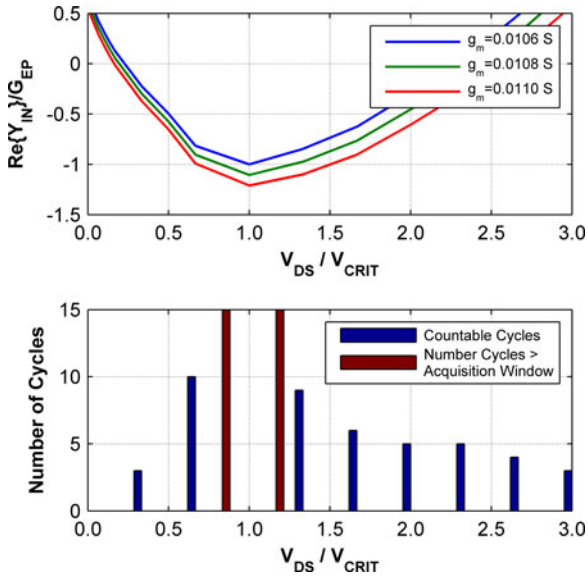

Fig. 10. Comparison of simulation output and empirical results. The top subplot shows simulation output and the bottom subplot shows histogram of empirical results. Parameters used for simulation were $L_G = 100$ nH; $L_D = 300$ nH; $G_{\mathrm{EP}} = 1.25$ mS; $C_2 = 900$ pF; and $R_{G\_\mathrm{NORM}} = 0.068$.

current. The drain current sensitivity will be addressed quantitatively in a separate paper but suffice to say here that the drain current influences the displacement current through the Miller capacitor at turn-off, and this in turn influences the initial condition of the gate inductor L_G at the end of the driven portion of the turn-off event.

Once the initial conditions for ensuring an initial V_{GS} ring-back could be replicated across a wide range of V_{BUS} values, a set of tests was run to evaluate the predictive utility of the small-signal model. The results of these tests are shown in Fig. 10 along with the conductance curves obtained from the small-signal model. It can be seen in this figure that sustained oscillations were experimentally observed at the bus voltage range for which the model using a small spread of g_m predicts a conductance ratio of approximately –1. It is also notable that the model predicts a gradual change of conductance on the high-voltage side and a rapid change in conductance on the low-voltage side. These predictions are also confirmed by the rapid change in the number of oscillations on the low-voltage side and a slower change in the number of oscillations on the high-voltage side. All model parameters except g_m were directly measured and were used to populate the simulation. The value of g_m was used as a fit parameter, since it wasnot known precisely, but the curve-fit value of 10.8 mS is consistent with curve tracer measurements made near the device's threshold voltage. The abscissa in these plots is normalized by the voltage at which the minimum conductance is observed (V_{CRIT}). In simulation, V_{CRIT} is observed to vary from tens of volts to hundreds of volts depending on the values of L_D, L_G, and the capacitance ratio C_2/C_1. Exemplary experimental waveforms corresponding to VDS/VCRIT values of 0.33, 0.83 and 3.0 are given in Fig. 11. It should be noted that the number of oscillations visible in each of these plots is in agreement with the histogram value shown in Fig. 10 for the corresponding operating condition.

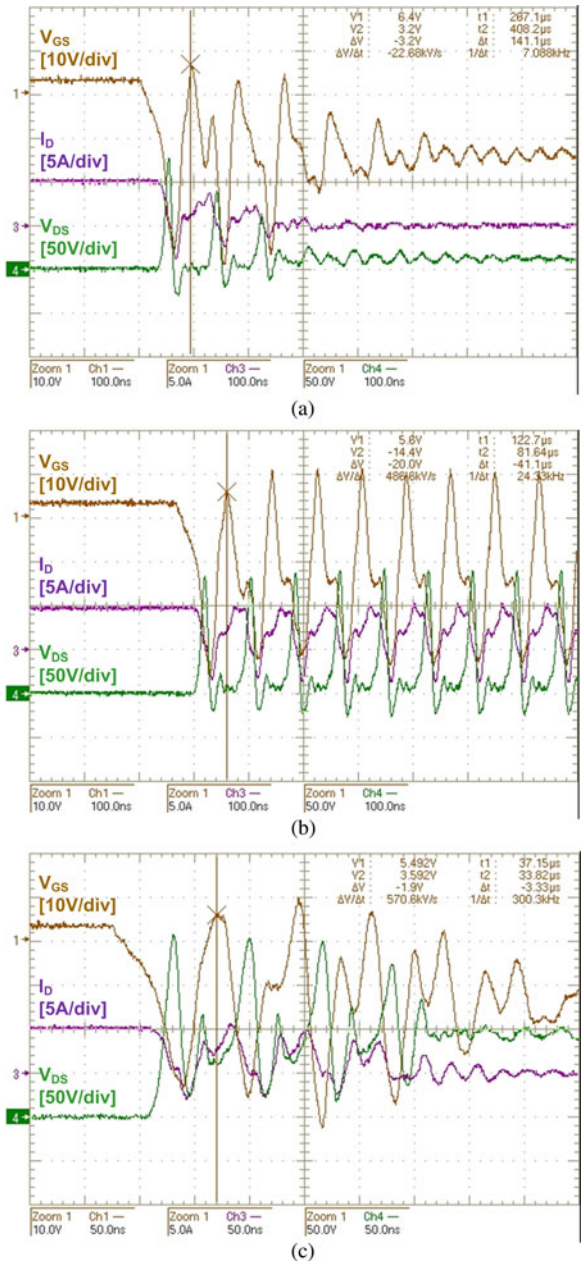

Fig. 11. Exemplary experimental waveforms corresponding to the histogram shown in Fig. 10. Subplots (a) and (c) demonstrate the occurrence of limited oscillation at $V_{\rm DS}/V_{\rm CRIT}$ values of 0.33 and 3.0, respectively. Subplot (b) demonstrates the occurrence of sustained oscillation at a $V_{\rm DS}/V_{\rm CRIT}$ value of 0.83.

IV. Practical Design Considerations

An understanding of the conditions under which sustained oscillations are possible can lead to a set of practical guidelines to discourage this phenomenon from occurring in power electronics applications. For example, it was shown in the discussion on initial conditions that the occurrence of this phenomenon is predicated upon a preliminary ring-back in the gate loop. This ring-back is caused by nonnegligible stray gate inductance L_G resonating with the switch input capacitance. The first effort in reducing the possibility of sustained oscillation, therefore, should be to reduce the stray gate inductance as much as possible. It should also be noted that a low gate resistor value ($<0.5\ \Omega$) is frequently used in half-bridge configurations to help prevent shoot-through by clamping the gate to the output of the gate-drive circuit. However, a low value of R_G tends to exacerbate the forced oscillation problem since it ensures that the gate loop is underdamped. It is possible to increase the gate resistor to reduce the possibility of sustained oscillation; however, this will result in reduced switching speed and increased losses. One alternative approach which is not subject to this tradeoff is the addition of a physical capacitor in parallel across the gate–source terminals of the FET. This must be done very close to the die, or the positive effects of the additional capacitance will be diluted by the presence of series stray inductance. This added capacitance has the effect of moving the critical voltage lower, where it usually does not result in sustained oscillation due to lower associated drain current. Increasing gate–source capacitance also helps reduce the likelihood of shoot-through because it increases the amount of charge required to bring $V_{\rm GS}$ to threshold, at the obvious cost of increasing the gate charge required to transition the switch ON or OFF. The addition of external gate–source capacitance as close to the semiconductor chip as possible, along with a small amount of gate resistance, is an effective strategy for improving the stability of the SiC FET-based half-bridge.

V. Conclusion

Silicon carbide field-effect devices present an opportunity for increased efficiency in power electronics applications. However, the near-ideality of these devices which makes this efficiency possible can also lead to the occurrence of oscillatory phenomena in these same applications. One of the most troublesome of these phenomena is the occurrence of sustained oscillations of the FET at turn-off, which can be observed with single devices in (for example) TO-247 packaging, but more often in multichip modules. This letter has presented an analytical treatment of this phenomenon on the basis of recognizing the power SiC FET and a minimal set of three parasitic components associated with the gate and drain circuits as an unintended negative conductance oscillator. In the context of established oscillator design theory, it has been shown both analytically and with simulation that negative differential conductance exhibited by the parasitic model explains the conditions under which instability is likely and empirical results corroborate this treatment. This letter also provides practical suggestions to aid application designers who may encounter this problem. Future work will report an analytical treatment of the initial conditions required for enabling the first oscillation to ring-back to threshold. Advanced methods are being developed for addressing this phenomenon in cases where the basic mitigation steps presented here are insufficient or impracticable.

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