Diode-Free Synchronous Rectification using a SiC Trench JFET

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Abstract

The reverse conduction mode of operation of the SiC trench JFET allows for diode-free synchronous rectification. This paper shows that the reverse conduction mode is an inherent property of the device caused by diffusion of electrons through the source fingers under conditions of moderate gate-drain diode forward bias. Experimental results confirm the expectations for a vertical-channel SiC JFET without internal body diode or external anti-parallel diode in a synchronously rectified buck converter switching 1.5 A at 200 V. Utilizing this mode minimizes the silicon-carbide die area and lowers component count for reduced total system cost.

1. Introduction

Synchronous rectifiers utilize transistors with low $R_{DS(ON)}$ and reverse conduction capabilities in order to eliminate freewheeling diodes with higher forward voltage drops for reduced power loss. The SiC trench JFET is known for its superior switching speeds, low specific on-resistance, and absence of an intrinsic body diode. Reverse conduction characterization of the normally-on SiC trench JFET shows nearly symmetric conduction at identically fast switching speeds. However, if dead time is used between switching off one transistor and switching on the second transistor in, for example, a half-bridge circuit, a diode is traditionally used to commutate freewheeling current.

In certain applications designers may use the intrinsic body diode of a silicon MOSFET [1] or silicon carbide MOSFET [2]. In others, an external diode is required; for example, when switching with IGBTs [3]. The vertical channel SiC JFET is a unique device in that two options other than an external diode are available to commutate current before gating the active rectifier is completed. The cascode form of the SiC JFET made from a high-voltage normally on SiC JFET and a low-voltage silicon MOSFET has been commercialized [4]. But in [5] it was first reported while studying the application of the *directly driven* (i.e., non-cascoded) normally off trench SiC JFET in a synchronous rectifier that the reverse conduction properties of the trench JFET can be utilized to free-wheel without an anti-parallel diode. This effect was first explained in [6] in behavioural terms as unipolar reverse conduction during mild forward bias of the gate-drain diode. In this paper, an explanation pointing to the lower potential barrier from the drain to the channel formed by the source finger as compared to diffusion across the drain-gate junction is documented, and an application example of this effect reported. This mechanism is usable in both the normally on and the normally off SiC trench JFET and does not require a cascoded silicon MOSFET. Utilizing this mode of operation minimizes the silicon-carbide die area and lowers component count for reduced system cost.

2. Device of Operation

Conventional understanding of ‘reverse conduction’ of a switch assumes a gate bias is applied such that a transistor is ‘turned on’ allowing the channel to conduct reverse current with a low $R_{DS(ON)}$. Other technologies that include an intrinsic body diode structure may conduct reverse current through the body diode while the switch is biased off. The normally-on SiC trench JFET allows for a “body diode like” mode of reverse conduction without the presence of an intrinsic body diode. In this mode of operation the gate is biased off with a negative voltage; typically V_{GS} = -15 V. If the drain voltage becomes negative with respect to the source potential, the voltage across the gate-drain junction will instead control the

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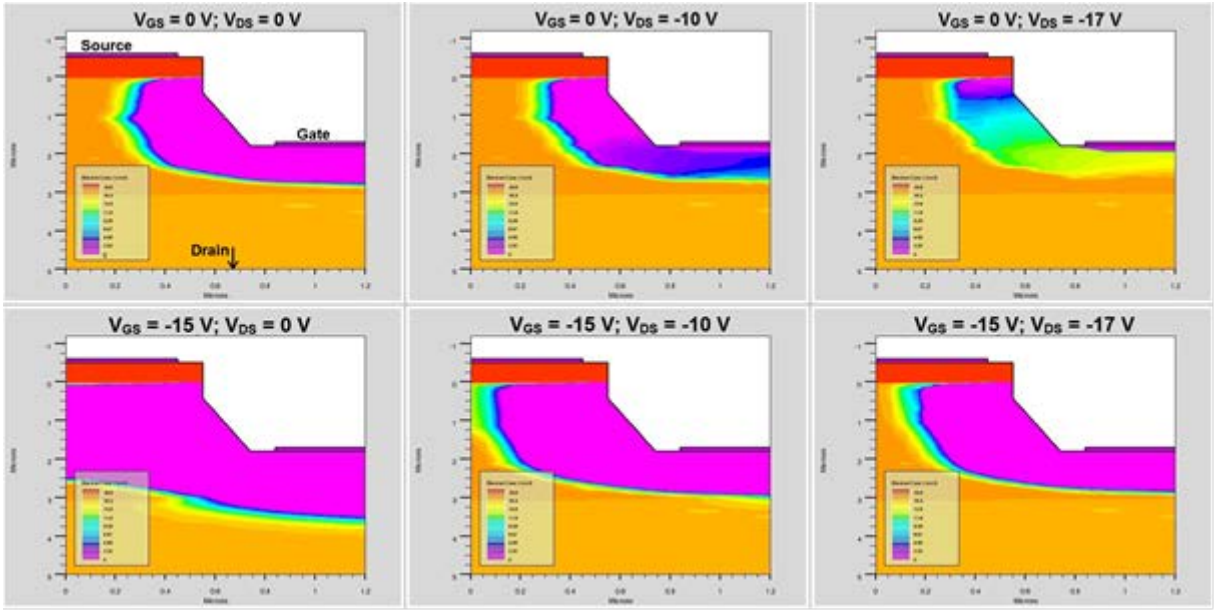

Figure 1. Electron concentration simulation for a normally on trench JFET channel with half symmetry. Orange color coding is for electron concentrations > 10^{16} cm^{-3}. Violet coloring is essentially fully depleted. The source contact is on top while the p-gate is to the right side. The drain is down and out of the image. Two views are provided for each drain-source voltage: top is for gated "on" operation (V_{GS} = 0 V) while bottom is for gated "off" operation (V_{GS} = -15 V). In the top case, the channel conducts for all V_{DS}. In the bottom case, the channel progressively becomes conductive as V_{DS} decreases. In (a) the channel either is conductive or not conductive depending on gate-source bias. But in (b) the threshold for conduction is reached at approximately the pinch-off voltage (V_{GD} = -5 V). By (c) the channel is in ohmic conduction with V_{GD} = 2 V.

channel. Since the gate-drain built-in potential is nearly the same as the gate-source built-in potential, diffusion current from the drain to the gate will begin to flow once $V_{GD} > 0$. By Kirchhoff's voltage law, this is satisfied when $V_{GS} - V_{DS} > 0$, i.e., V_{DS} must be more negative than V_{GS}. However, external to the device, it is not immediately obvious where the preponderance of electrons surmounting the potential barrier will flow.

Figure 1 provides an electron concentration simulation of the SemiSouth SJDP120R085 for two different constant gate biases (V_{GS} = 0 V and -15 V) and three negative drain potentials (V_{DS} = 0 V, -10 V, -17 V respectively). As shown in Fig. 1a the channel is completely pinched off by the negative gate-source bias. As V_{DS} becomes more negative electrons clearly begin to fill the channel as shown in Fig. 1b. At V_{DS} = -17 V V_{GD} increases toward V_{bi} for 4H-SiC and in Fig. 1c the channel is not pinched off but is in ohmic conduction instead. The mechanism for this conduction is preferential diffusion across a lower potential barrier in the JFET channel between the p-gates. Electrons diffusing across the barrier then drift down the potential barrier in the source finger where they are collected at the source contact. This deposits kinetic energy in the channel which externally appears as a power loss equal to the product $V_{GS} \cdot I_S > 0$, where I_S is the source current. The greater the negative bias applied to the gate with respect to the source, the greater the power dissipation in the channel while operating in this conduction mode. Therefore, it is essential that the conduction mode only be used for dead time commutation and that the dead time be minimized.

Two factors favor such optimal operation. First, dead time for unipolar devices is shorter than for bipolar devices, where tail current is the principle justification for dead-time switching. A second practical reason is that using diffusion to establish the load current in the channel of the JFET used as the synchronous rectifier is a one-step commutation process. This eliminates problems with unclamped inductance when commutating the current from the intermediate path, such as an external diode, during the two-step commutation sequence

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required by virtually all other competing device types, including the SiC MOSFET because the body diode is not a desirable free-wheeling rectifier [7].

3. Application Example

Figure 2 shows a buck converter application based on SiC trench JFETs without anti-parallel diodes. The low-side switch is a synchronous rectifier where the dead time is about 100 ns. Figure 3 shows the typical result of switching this half-bridge with a bus voltage of 200 V and a load current of 1.5 A. All three stages of conduction are observable. J2 begins the cycle blocking forward conduction. At the moment that J1 begins switching off, the resulting dV/dt is imposed on J2 with a collapse of the drain-source voltage in 30 ns. The drain current swings negative to the load value of 1.5 A, reflecting commutation of the current through inductor L from J1 to J2. J2's V_{DS} also swings negative to approximately equal V_{GS} until the gate driver switches V_{GS} to slightly positive bias. As a result of this gate-drive action, the drain current does not change but J2's V_{DS} collapses to nearly zero as expected from a switch biased to conduct. In other tests not reported here, a 600 V bus was similarly switched in a double-pulse clamped inductive load test.

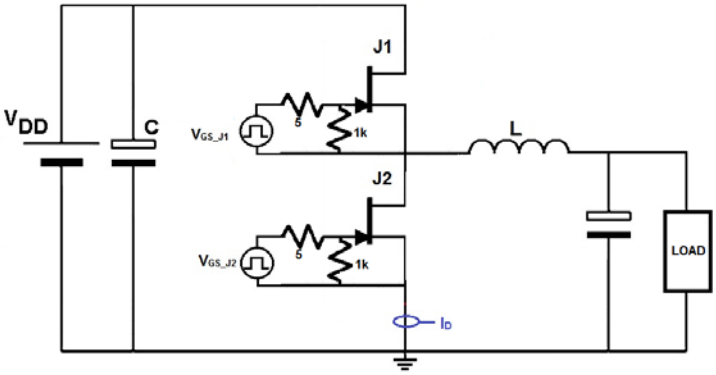

Figure 2. Half bridge circuit for measuring he freewheeling behavior of a reverse conducting SiC trench JFET that does not have an intrinsic body diode.

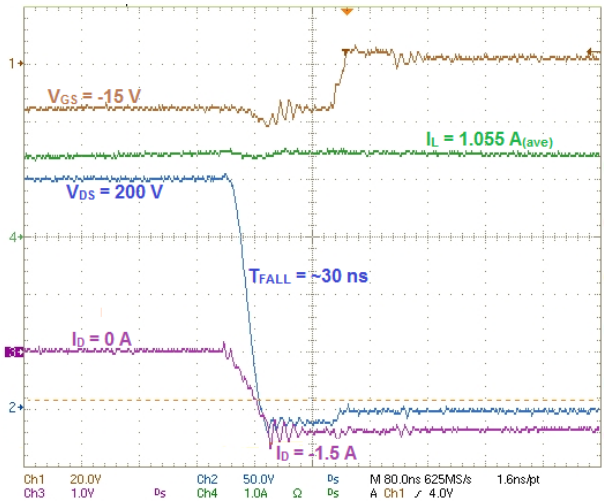

Figure 3. Reverse conduction waveforms for transistor J2 of the buck converter shown in Fig. 2. In the figure, I_L = 1.55 A.

4. Discussion

The vertical channel "trench" JFET is a unipolar device without an intrinsic body diode [5]. However, conduction through the channel is inherently symmetrical, and the properties of the gate-source diode and the gate-drain diode which form the device structure are also nearly

symmetrical. This means that the threshold or pinch-off voltage conditions apply to either diode. Thus, the trench JFET is inherently self-protecting in that reverse potential beyond that applied to the gate-source diode is not possible as the gate-drain diode will become forward biased. Dangerous current flowing into the gate drive is prevented by the channel, which as shown in Fig.1 will conduct the current instead.

Alternatively, if an external diode is provided in anti-parallel with the JFET, then a coercive potential up to the applied reverse bias on the gate-source diode will prevent channel conduction and instead forward bias the anti-parallel diode into conduction. This will allow easy commutation of current to the free-wheeling rectifier in anti-parallel for 100% utilization of the free-wheeling rectifier active area, a feature that is otherwise not possible with the alternative unipolar device: the MOSFET [7].

Thus, the trench SiC JFET gives unprecedented options to the circuit designer for managing reverse current commutated to the blocking switch during dead time in clamped inductively loaded applications. These options range from a minimally sized anti-parallel diode for maximum economy, to equivalently rated anti-parallel diode for maximum efficiency. Efficiency and economy can be optimized for each application in a way unavailable from any other comparable device.

5. Conclusion

The “body diode like” mode of reverse conduction possible with SiC trench JFETs provides designers a new option for synchronous rectification that encourages high switching frequencies, low part count, and reduced total system cost; and in particular, the smallest total SiC die area available to the system designer.

6. References

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