A Scalable SiC Device for DC/DC Converters in Future Hybrid Electric Vehicles

Robin Kelley[1], Michael S. Mazzola[1], and Volodymyr Bondarenko[2]
[1]SemiSouth Laboratories, Inc., 200 Research Blvd., Starkville, MS 39759
[2]Center for Advance Vehicular Systems (CAVS),
Mississippi State University, 201 Research Blvd., Starkville, MS 39759

Abstract— The potential increased power density and high temperature capability of silicon carbide makes it an ideal candidate for use in future hybrid electric vehicle (HEV) technology. A secondary cooling system is required to maintain an 85°C base plate temperature for silicon based power electronics; but by creating a silicon carbide (SiC) based replacement this requirement could be relaxed. One anticipated benefit, among many, is that the secondary cooling loop could be eliminated and instead interfaced with the engine coolant system designed to maintain a maximum temperature of 105°C. The purpose of this paper is to present an all-SiC scaled prototype that is modeled after the DC-DC converter used in the Prius II to establish a high voltage DC bus interconnecting the motor and generator. The design uses a SiC JFET and SiC Schottky diode as the switching pair of a 1 kW scale model that investigates an inherently safe approach for use in future HEVs. The ability to parallel these unipolar devices results in a scalable device technology capable of achieving high-current, 600-V SiC switch technology in the near term that offers a potential 100°C increase in junction temperature above that rated for comparable silicon IGBTs.

I. INTRODUCTION

This work is motivated by an industry wide interest to integrate SiC power devices in future automotive applications. The need to mount electric motor drives and other power converter electronics under the hood and as close to the motor as possible demands that the power electronics installed must either be capable of enduring the high under-hood temperatures or incorporate an extra cooling system. The use of SiC power device in under-hood power electronics would allow for more relaxed cooling requirements, elimination of a second cooling system, and integration with the current motor coolant system. The ability to reduce the necessary cooling mechanisms and overall package design is what will balance out the higher cost of using SiC devices over silicon in future automotive electronics.

Fig. 1 provides a block diagram of the high voltage system used in the current Toyota Prius HEV. Within the Prius a 200V battery bank is established by connecting several individual batteries in series. In the first generation vehicles, original Prius, this 200V battery voltage was used to directly drive the electric motor. In the second generation vehicles, Pruis II, a high voltage power converter was included to boost this voltage to create a 500-V bus voltage for the motor/generator. While the power

electronics in a modern "hard" HEV power train, such as the system in the Toyota Prius II, is typically rated for 50 kW, a scaled prototype was designed and fabricated to investigate gate driver design to provide initial results that show the feasibility of SiC in HEV power electronics.
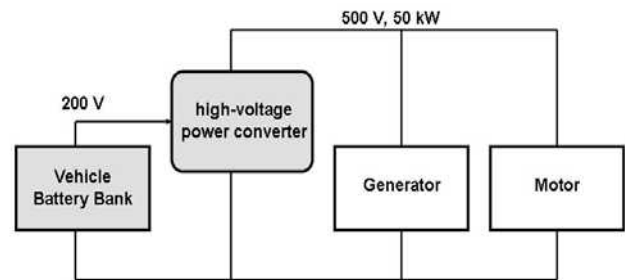

Fig. 1. Block diagram of the high voltage system in the Toyota Pruis

II. CONVERTER DESIGN AND RESULTS

A classic boost converter was designed to deliver roughly 1 kW of continuous power, operating at 100 kHz, and using SiC devices as the switching pair. This prototype boosts an input voltage of 200 V simulating minimum battery bank voltage to an output voltage of 500 V, the regulated DC bus voltage within the Prius II [1]. Even though the JFET is generally thought of as a normally on device, SiC JFETs can be fabricated and practical gate drivers designed to support JFETs with less negative, or even positive, threshold voltage. Such devices can exhibit an ideal combination of enhancement mode functionality, similar to conventional normally off silicon devices, with the advantage of bias-enhanced blocking voltage unique to the JFET that permits higher blocking voltage and lower on-resistance [2]. In a conventional boost converter, as well as many types of resonant converters, enhancement mode functionality and bias-enhanced blocking greatly simplifies the gate driver and start up circuit design such that SiC JFET converter has essentially the same safety as a converter switched with a purely normally off silicon switch. This is because many converters, including the boost converter considered here, stress the switch at two different characteristic voltage levels: a static or dc voltage level, and a higher dynamic voltage level. If the SiC JFET is

rated to block the lower dc value at $V_{GS} = 0$ V, and the gate driver is designed to supply the small negative gate-source bias voltage (say $V_{GS} \leq$ -3 V) necessary for the JFET to block the higher dynamic voltage, an inherently safe design results because the higher dynamic voltage can only exist if the converter, including gate-drive circuitry, is working properly. Typically, the enhancement-mode JFET can block 50% of rated voltage (~300 V) at $V_{GS} = 0$ V, and 100% of rated voltage (600 V) with $V_{GS} \leq$ -3 V. Fig. 2 provides evidence of the enhancement mode blocking capabilities in a typical BV_{DS} vs V_{GS} curve.
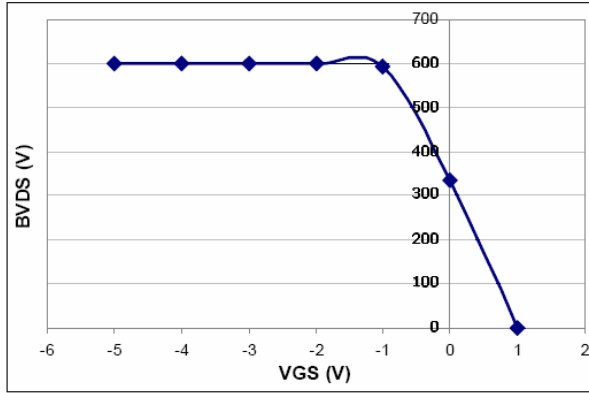

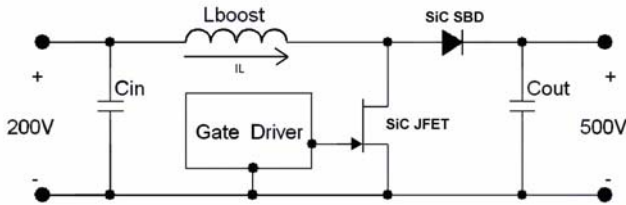**Fig. 2.** BV_{DS} vs V_{GS} curve for Bias Enhanced SiC JFET.

Fig. 3. HEV boost converter solution made with a SiC JFET and SiC SBD.
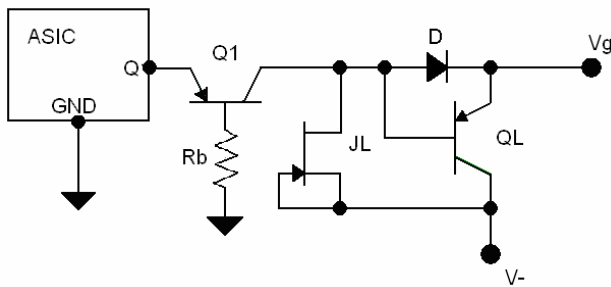

Fig. 4. Gate driver using standard ASIC controller.

The core boost converter, as shown in Fig. 3, was designed according to standard approaches found in the literature [3]. The circuit shown in Fig. 4 is an effective solution for interfacing a SiC JFET with a standard commercially available ASIC controller. Voltage V– is a low-voltage rail derived from an auxiliary winding on the boost inductor; thus dynamic charging of the output capacitor, the source of the dynamic voltage stress on the JFET while the freewheeling diode is conducting, must also charge the capacitor supporting the V– voltage bus. Since the output of the ASIC typically varies between GND and V_{CC}, a totem pole is used to level shift the output control pulse to provide the dynamic gate-source voltage pulse ranging between $V_{GS} \approx$ +3 V (necessary for turn-on), and $V_{GS} \approx$ V- (necessary to block the dynamic voltage stress while the freewheeling diode is conducting). The JFET requires minimal gate-drive current; therefore, the ASIC is capable of sourcing and sinking the typical gate currents needed to drive a modest number of SiC JFETs in parallel. Thus, Fig. 4 incorporates the use of a bypass diode D in place of the high-side NPN transistor otherwise found in the typical totem-pole output buffer. In a fully scaled SiC switch rated in the several hundreds of amperes and consisting of a large number of paralleled JFET die, a higher gate current may be required, in which case the bypass diode is replaced with a high-side NPN transistor supplied by V_{+}, a positive rail voltage equal to the +3 V required for turn on.

The results for the prototyped boost converter operating at 1 kW are shown in Fig. 5. Again the prototype was modeled after the boosting requirements of the high voltage power converter required in the high voltage system for the Toyota Prius II as shown in Fig. 1. The prototype successfully boosted a 200 VDC input to establish a regulated 500 VDC voltage bus while maintaining a total output power of 1 kW, and operating at > 90% efficiency. Fig. 5 provides an oscilloscope capture of the critical waveforms for the boost converter, V_{IN}, V_{DS}, V_{GS}, and I_L. Fig. 6 provides a zoomed view of the drain-source voltage, gate-source voltage, and boost inductor current in order to illustrate the excellent switching characteristics of the SiC power devices and the gate driver circuit which aids to further reduce switching losses by providing a very fast switching drive signal. The 100 kHz switching frequency is no challenge for the SiC switching pair, JFET and Schottky barrier diode. This figure also illustrates the two levels of voltage stress that the switch must be able to withstand (static stress: $V_{in} = 200$ V DC, dynamic stress: $V_{DS(peak)} = V_{out} = 510$ V).

This is an excellent application for the bias-enhanced SiC JFET presented in previous work [2] and revisited at the beginning of this section, Fig. 2. By using a bias-enhanced SiC JFET, inherently safe operation is provided in the case of a gate driver by the characteristic enhancement mode functionality of this particular device. At start-up and during any driver failure event the switch is capable of blocking the full DC input voltage indefinitely as if it were any other normally off device. Once switching is initiated a

negative bias is derived to allow the switch to block to the higher voltage dynamic stress created during normally boosting action. Therefore, as long as the converter is operating according to normal behavior a negative bias is present for blocking high voltages. If the gate driver were to unexpectedly fail, normal switching behavior would cease, the dynamic stress would die down, at which time the derived negative bias would begin to discharge, and the switch would only be required to block the input DC voltage again which it is certainly capable of doing at $V_{GS} = 0V$ as illustrated in Fig. 2.
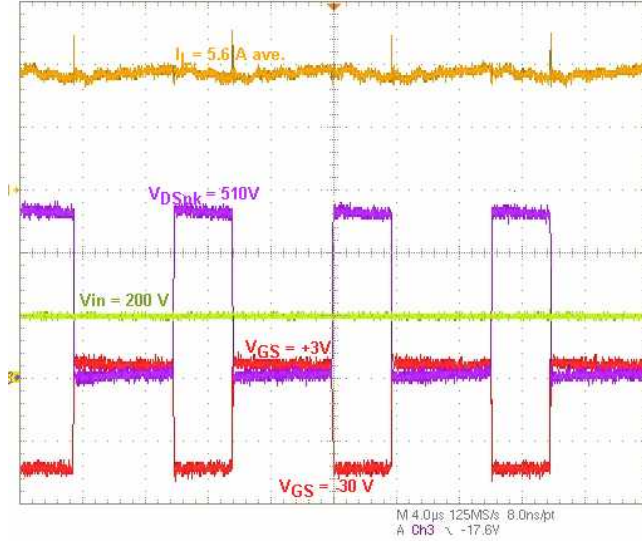

Fig. 5. Oscilloscope traces of V_{IN}, V_{DS}, V_{GS}, and I_L for $P_{out} = 1$ kW and $f_s = 100$ kHz.
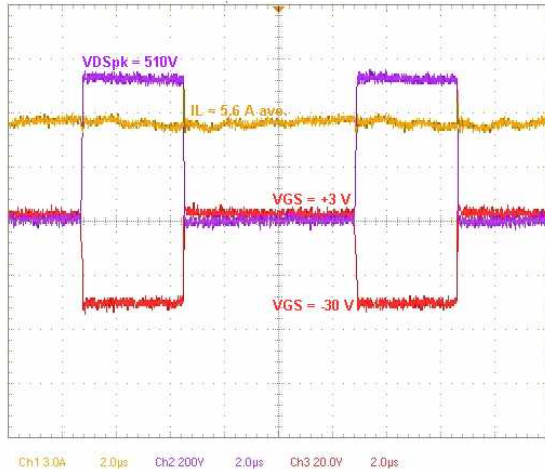

Fig. 6. Zoomed view of a single switching transient to show the fast switching behavior of the SiC JFET.

III. SCALABILITY

VJFETs in SiC are especially attractive for high power and high temperature applications because of the inherent stability of the p-n junction gate and the basic maturity of all aspects of the JFET technology in SiC. While individual VJFET devices are applicable to kilowatt-class power supplies requiring 5- to 10-A, 600-V or 1200-V ratings, the 100% unipolar structure allows multiple die to be easily paralleled in order to form an equivalent switch capable of much greater current ratings. The paralleling of several small JFET die together in a single package produced the SiC switch used in this prototype. Each 600-V die is rated for 5 A at $V_{DS} = 5$ V and $V_{GS} = 3$ V. Paralleling additional die until an acceptable on-state conduction loss was achieved increased the efficiency. Nine devices were paralleled in order to produce a device that could conduct 5 A, the average input of the 1-kW design, at $V_{DS(on)} = 0.3$ V. The efficiency at 500 W is at least 98%. In a previous report [4], this process was repeated by paralleling five larger area devices in order to produce a fast switching 150-A device; package shown in Fig. 7 with a fast switching behavior illustrated by the single switching event shown in Fig. 8. This provides evidence that a "drop-in" replacement for the silicon IGBT switches used in HEV converters and motor drives, but with a much higher rated junction temperature, is a relatively simple extension of this work.
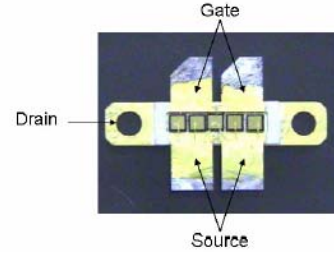

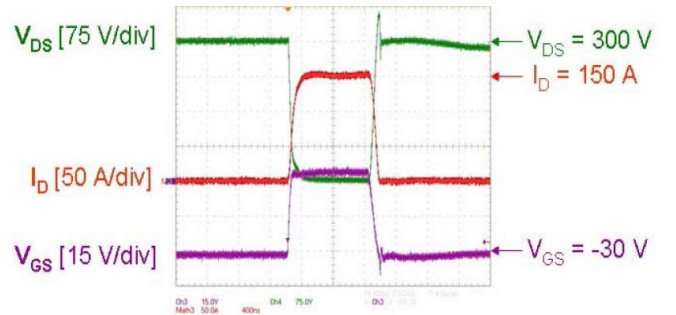**Fig. 7.** 150-A SiC JFET composed of 5 parallel die.

Fig. 8. Performance of a 600-V, 150-A SiC VJFET switch fabricated with five parallel die. This switch is capable of a maximum operating frequency of 6 MHz.

IV. CONCLUSION

A pure SiC VJFET switch and SiC Schottky diode pair demonstrated fast switching and high-efficiency at 1 kW in a boost-type voltage converter patterned after the power electronics found in the Toyota Prius II. Scalability has also

been addressed by paralleling multiple devices in order to achieve a higher current rated equivalent switch made from several lower rated devices. This provides evidence that a resulting scaled switch can be developed that is suitable for a full scale 50 kW design such as that used in the Prius. While this would allow for a high frequency, high efficiency design, the silicon carbide is also capable of operation at the elevated under-hood temperatures. This would allow for the elimination of a second cooling system and the possible integration with the current motor coolant system. Also, this work demonstrates that a resulting scaled switch could be developed that meets the average and surge current ratings comparable to a silicon IGBTs while exhibiting switching properties like silicon MOSFETs. However, the equivalent SiC VJFET-based switching module will have lower thermal resistance and higher rated junction temperature than any available silicon devices due to the thermal properties of the silicon carbide. This resulting switch could then be used to redesign the motor drive power electronics as well as the high voltage bus regulator presented here.

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